Scientific & Technical Information Center
S T I C
USPTO

STIC Search Report
EIC 2800

STIC Database Tracking Number 137043

TO: David Hogans
Location: JEF-7D30
11/17/2004
AU 2813
Case Serial No. : 10/604,246

From: Jeff Harrison
Location: STIC-EIC2800
JEF-4B68
Phone: 22511

Email: harrison, jeff

Search Notes

Dear Examiner Hogans,

Re: RTA, comparing measured value with preset range, end the RTA

Attached are edited results from subject-searching in the patent literature.

I tagged a few items worth your review, but I suggest that you browse the entire stack of results.

If you'd like additional searching or explanation, let me know.

Respectfully,
Jeff Jeff

Jeff Harrison
Team Leader, STIC-EIC2800
JEF-4B68, 571-272-2511

STIC Search Results Feedback Form

EIC 2800

Questions about the scope or the results of the search? Contact ***the EIC searcher or contact*:**

Jeff Harrison, EIC 2800 Team Leader
571-272-2511, JEF 4B68

Voluntary Results Feedback Form

- *I am an examiner in Workgroup:* ☐ *Example: 2810*
- *Relevant prior art* ***found****, search results used as follows:*
  - ☐ 102 rejection
  - ☐ 103 rejection
  - ☐ Cited as being of interest.
  - ☐ Helped examiner better understand the invention.
  - ☐ Helped examiner better understand the state of the art in their technology.

  Types of relevant prior art found:
  - ☐ Foreign Patent(s)
  - ☐ Non-Patent Literature
    (journal articles, conference proceedings, new product announcements etc.)
- *Relevant prior art* ***not found:***
  - ☐ Results verified the lack of relevant prior art (helped determine patentability).
  - ☐ Results were not useful in determining patentability or understanding the invention.

Comments:

Drop off or send completed forms to STIC/EIC2800, CP4-9C18

sira
Search and Information Resources Administration

137043

STIC EIC 2800
Search Request Form

Today's Date: Nov. 3, 2004

What date would you like to use to limit the search?

Priority Date: July 4, 2003 Other:

Name David Hogans

AU 2813 Examiner # 79069

Room # Jef 7D30 Phone 272-1691

Serial # 10/ ~~602~~ 604, 246

Format for Search Results (Circle One):

PAPER DISK EMAIL

Where have you searched so far?

USPAT DWPI EPO JPO IBM TDB

IEEE INSPEC Other

Is this a "Fast & Focused" Search Request? (Circle One) YES NO

Please request a "Fast & Focused" search in-person at EIC2800, JEF-4B68. A "Fast & Focused" Search is completed in 2 hours (maximum). The search must be on a very specific topic and meet certain criteria. The criteria are posted in EIC2800 and on the EIC2800 NPL Web Page at http://ptoweb/patents/stic/stic-tc2800ffcriteria.htm

What is the topic, novelty, motivation, utility, or other specific details defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, definitions, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract, background, brief summary, pertinent claims and any citations of relevant art you have found.

Please Search Claim 15

11-04-04 A09:12 IN

Keywords:

RTA or RTP or (rapid with thermal)

compar#4 or measur#3

variable or parameter or temperature

preset#4 or predetermind or fixed

terminat#3 or stop#4 or end#5 or halt#3

Crux of Invention:

comparing a measured temperature value of a substrate ~~with~~ against an acceptable temperature range, and if temperature is too high, the annealing process is terminated.

Thank you

STIC Searcher HARRISON Phone 22511

Date picked up 11/15/04 Date Completed 11/17/04 Dialog

16nov04 15:42:16 User259284 Session D2967.10

File 342:Derwent Patents Citation Indx 1978-04/200471
(c) Thomson Derwent

```
      Set  Items  Description
      ---  -----  -----------
Executing SD747
      S1       0  Serial: SD747
      S2       1  PN='WO 200022655'
? map ct
1 Select Statement(s), 4 Search Term(s)
Serial#SD748
Executing SD748
      S3      33  Serial: SD748
? map pn temp
6 Select Statement(s), 57 Search Term(s)
Serial#TD278
```

```
       16nov04 15:43:48 User259284 Session D2967.11
SYSTEM:OS  - DIALOG OneSearch
  File 350:Derwent WPIX 1963-2004/UD,UM &UP=200473
  File 347:JAPIO Nov 1976-2004/Jul(Updated 041102)
  File 344:Chinese Patents Abs Aug 1985-2004/May
  File 348:EUROPEAN PATENTS 1978-2004/Nov W01
  File 349:PCT FULLTEXT 1979-2002/UB=20041111,UT=20041104
Executing TD278
              16  PN=AU 200020416 + PN=AU 200125345 + PN=AU 200176882 +
                  PN=DE 10146307 + PN=DE 19652124 + PN=EP 1127369 + PN=EP
                  848244 + PN=EP 883857 + PN=EP 950180 + PN=GB 2358702 +
                  PN=JP 10275885 + PN=JP 11238656 + PN=JP 2001507803 +
                  PN=JP 2001524228
              11  PN=JP 2003515914 + PN=JP 2881418 + PN=KR 2001080190 +
                  PN=TW 432452 + PN=TW 512450 + PN=US 2002069972 + PN=US
                  5940681 + PN=US 5953130 + PN=US 5960125 + PN=US 5974169 +
                  PN=US 5978080 + PN=US 5978502 + PN=US 6026176 + PN=US
                  6067379
              14  PN=US 6075881 + PN=US 6137893 + PN=US 6141033 + PN=US
                  6215915 + PN=US 6218199 + PN=US 6236769 + PN=US 6282328 +
                  PN=US 6298149 + PN=US 6301396 + PN=US 6352422 + PN=US
                  6381366 + PN=US 6381375 + PN=US 6396949 + PN=US 6415977
              24  PN=US 6442291 + PN=US 6587582 + PN=US 6684402 + PN=US
                  6687402 + PN=US 6705925 + PN=US 6719550 + PN=US 6748104 +
                  PN=WO 200022655 + PN=WO 200034918 + PN=WO 200155963 +
                  PN=WO 200235585 + PN=WO 9818117 + PN=WO 9830890 + PN=WO
                  9852349
               3  PN=WO 9915864
              50  S1:S5
      S1      50  Serial: TD278
      S2      11  S1 AND (COMPARI????????? OR COMPARE??????????)
      S3       8  S1 AND MEASUR???????????
      S4       1  S1 AND PYROMETER? ?
      S5       6  S2 AND S3:S4

S6         14   PN=DE 19652124 + PN=EP 848244 + PN=JP 10275885 + PN=US 5940681 + PN=WO 0022655 +
                PN=WO 0155963 + PN=WO 200022655 + PN=WO 200155963 + PN=WO 9818117 + PN=WO 9915864
S7         21   S2:S6
S8     207333   MEASUR????????(3N)(VARIABLE? ? OR PARAMETER? ? OR CONDITION? ? OR TEMPERATURE? ? OR
POWER? ?)
S9      71157   (COMPARI????????? OR COMPARE??????????)(3N)(VARIABLE? ? OR
             PARAMETER? ? OR CONDITION? ? OR TEMPERATURE? ? OR POWER? ?)
S10     17460   8AND9
S11    110107   (COMPARI????????? OR COMPARE??????????)(10N)MEASUR????????-
             ?????
S12      8586   10AND11
S13       288   S12 AND IC=H01L
S14       895   S12 AND (RTA OR RTP OR ANNEAL??????? OR RAPID??(2N)THERMAL???????)
S15        79   13AND14
S16        79   S15 NOT S7
S17        76   S14 AND STOP???????/TI,AB,CM
S18        15   S14 AND HALT???????/TI,AB,CM
S19        49   S14 AND TERMINAT???????/TI,AB,CM
S20       117   S14 AND COMPLET????/TI,AB,CM
S21         5   S14 AND ABORT????/TI,AB,CM
S22        20   S16 AND S17:S21
S23        45   S23:S25
S24         6   S23 AND (RTA OR RTP)
S25        21   S23 AND ANNEAL??????
S26        20   S23 AND WAFER??
S27        29   S23 AND SEMICOND????????
S28        26   S23 AND SUBSTRATE
S29        20   S24:S25 AND S26:S28
S30        23   (COMPARI????????? OR COMPARE??????????) AND MEASUR?????????  AND S23
S31        28   S21 OR S24 OR S30
S32        30   S29 OR S31
S33        13   S32 AND (FURNACE? ? OR OVEN? ? OR RTA OR RTP OR THERMAL???-
             ???? OR ANNEAL??????? OR HEAT??????)/TI,AB
S34         5   S33 AND WAFER? ?
```

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? b 6 8 315
      16nov04 16:29:28 User259284 Session D2967.14

SYSTEM:OS  - DIALOG OneSearch
  File   6:NTIS 1964-2004/Nov W1
         (c) NTIS, Intl Cpyrght All Rights Res
  File   8:Ei Compendex(R) 1970-2004/Nov W1
         (c) Elsevier Eng.  Info. Inc.
  File 315:ChemEng & Biotec Abs 1970-2004/Oct
         (c) DECHEMA

Set     Items   Description
S1         29   (ABORT??????? OR INTERRUPT?????? OR END??????? OR STOP????-
             ?? OR HALT??????? OR TERMIN???????)(5N)(RTP OR RTA)
S2        454   (ABORT??????? OR INTERRUPT?????? OR END??????? OR STOP????-
             ?? OR HALT??????? OR TERMIN???????)(5N)ANNEAL????????
S3       3962   (ABORT??????? OR INTERRUPT?????? OR END??????? OR STOP????-
             ?? OR HALT??????? OR TERMIN???????)(5N)HEAT???????
S4       2733   (ABORT??????? OR INTERRUPT?????? OR END??????? OR STOP????-
             ?? OR HALT??????? OR TERMIN???????)(5N)THERMAL???
S5         82   (ABORT??????? OR INTERRUPT?????? OR END??????? OR STOP????-
             ?? OR HALT??????? OR TERMIN???????)(5N)OVEN??
S6        449   (ABORT??????? OR INTERRUPT?????? OR END??????? OR STOP????-
             ?? OR HALT??????? OR TERMIN???????)(5N)FURNACE??
S7          3   S1 AND S2:S6
S8          3   RD S7 (unique items)
S9        361   S1:S6 AND SEMICOND?????????
S10         9   1AND9
S11         7   S10 NOT S7
S12         7   RD S11 (unique items)
S13        38   S1:S6 AND ABORT??????????
S14       507   S1:S6 AND INTERRUPT?????????
S15      1554   S1:S6 AND TRANSFER???????
S16        40   S9 AND S13:S15
S17        39   S16 NOT (S11 OR S7)
S18        38   RD S17 (unique items)
```

16nov04 16:19:17 User259284 Session D2967.13

SYSTEM:OS - DIALOG OneSearch
File 34:SciSearch(R) Cited Ref Sci 1990-2004/Nov W2
(c) Inst for Sci Info
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
(c) 1998 Inst for Sci Info

Set	Items	Description
S1	214	CR=BARNA G?
S2	8	S1 AND (RTA OR RTP OR ANNEAL?????? OR RAPID?????(4N)(TEMPERATURE? ? OR HEAT?????? OR THERMAL??????? OR PROCESS???????))
S3	2	S1 AND (FURNACE? ? OR OVEN? ? OR HEATER? ? OR HEATING? ? OR HEATED)
S4	10	S2:S3
S5	560	CR=HERMAN IP?
S6	20	S5 AND (FURNACE? ? OR OVEN? ? OR HEATER? ? OR HEATING? ? OR HEATED)
S7	19	S5 AND (RTA OR RTP OR ANNEAL?????? OR RAPID?????(4N)(TEMPERATURE? ? OR HEAT?????? OR THERMAL??????? OR PROCESS???????))
S8	33	S6:S7 NOT S4
S9	9	S8 AND SEMICOND?????????????
S10	0	(S1 OR S5) AND ABORT???????
S11	0	(S1 OR S5) AND INTERRUPT???????
S12	2	(S1 OR S5) AND TERMINAT?
S13	0	(S1 OR S5) AND HALT????????
S14	85	(S1 OR S5) AND TRANSFER????????
S15	2	S14 AND S6:S7
S16	1	1AND5
S17	3	S15:S16

16nov04 16:01:15 User259284 Session D2967.12

File 2:INSPEC 1969-2004/Nov W1
(c) Institution of Electrical Engineers

Set	Items	Description
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Set	Items	Description
S1	164867	R1:R6 OR R9 OR R11 OR RTA OR RTP
S2	39232	R1:R3 OR R8 OR R12:R15
S3	780	1AND2
S4	107	S3 AND (STOP??????? OR END????? OR TERMIN????????? OR HALT-???????? OR FINISH??????? OR COMPLET??????? OR TRANSFER??????-?)
S5	40	S4 AND WAFER?????????
S6	52	S4 AND SEMICOND????????
S7	16	S4 AND (COMPARE????? OR COMPARI???????)
S8	59	S4 AND (MEASUR?????????? OR PYROMET???????)
S9	10	S5:S6 AND S7
S10	36	S5:S6 AND S8
S11	10	7AND8
S12	6	9AND10
S13	6	9AND11
S14	6	10AND11
S15	14	S9 OR S11:S14
S16	107	SETPOINT??/TI
S17	0	3AND16
S18	5	S16 AND PROCESS?????/TI
S19	747530	FUZZY CONTROL OR FUZZY NEURAL NETS OR CONTROL ENGINEERING - COMPUTING OR PROCESS COMPUTER CONTROL OR CONTROL SYSTEM SYNT-HESIS OR CONTROL?????/TI,DE,ID
S20	52016	PREDICTIVE CONTROL OR OPTIMAL CONTROL OR NEUROCONTROLLERS
S21	747802	S19:S20
S22	464	3AND21
S23	71	4AND21
S24	47	S5:S8 AND S23
S25	38	S24 NOT (S18 OR S15)
S26	30	S25 AND SEMICONDUCT???????????
S27	38	S25:S26
S28	2119	PROCESS????????(3N)(ABORT??????? OR TERMINAT?????? OR HALT-????? OR STOP??????)
S29	0	3AND28
S30	63	S1:S2 AND S28
S31	57	S24 OR S18 OR S15
S32	63	S30 NOT S31
S33	7	S32 AND WAFER? ?
S34	0	S32 AND MICROCHIP? ?
S35	1085	PROCESS????????(3N)(ABORT??????? OR TERMINAT?????? OR HALT-????????)
S36	48	(RTA OR RTP OR ANNEAL?????)(3N)(ABORT??????? OR TERMINAT??-???? OR HALT????????)
S37	5	35AND36
S38	1128	S35:S36
S39	115	S38 AND SEMICOND????????????
S40	62	S31 OR S37
S41	112	S39 NOT S40
S42	0	S41 AND SETPOINT????????
S43	14	S41 AND RANG???????
S44	2	S41 AND PARAMETER? ?
S45	16	S43:S44

16nov04 14:43:14 User259284 Session D2967.6

```
SYSTEM:OS  - DIALOG OneSearch
  File 348:EUROPEAN PATENTS 1978-2004/Nov W01
         (c) European Patent Office
  File 349:PCT FULLTEXT 1979-2002/UB=20041111,UT=20041104
         (c) WIPO/Univentio

Set      Items   Description
S1      139727   MEASUR????????(3N)(VARIABLE? ? OR PARAMETER? ? OR CONDITIO-
              N? ? OR TEMPERATURE? ? OR POWER OR VOLTAGE? ? OR CURRENT? ? OR
               RESISTANCE? ? OR RESISTIVIT????)
S2      105506   COMPAR?????(5N)(TARGET????? OR REFERENC?????? OR PREDETERM-
              IN????????? OR PRE OR PREVIOUS????? OR PRESET??????? OR PREES-
              TABLISHED??????? OR SETPOINT??? OR SET()POINT?? OR GOAL??)
S3       12205   COMPAR?????(4N)RANGE??
S4       10338   OOR OR OUT(2W)RANGE
S5       17547   COMPAR?????(3N)AGAINST
S6       41331   COMPAR??????(4N)(POWER?? OR TEMP OR TEMPS OR TEMPERATURE??)
S7        2112   PYROMETER? ?
S8       75073   IC=H01L?
S9        8449   RTP OR RTA OR RAPID??(2N)THERMAL????
S10      86541    (WAFER??????? OR CHIP? ? OR MICROCHIP? ? OR DICE OR DIES OR
               (SI OR SILICON OR SEMICONDUCT???????)(4N)(DIE OR SUBSTRATE? -
              ?))/TI,AB,CM
S11     178066    (OPERAT?????? OR PROCESS?????? OR ANNEAL????? OR RTA OR RTP
               OR RAPID??)(4N)(VARIABLE? ? OR TEMPERATURE? ?)
S12     162055   S2:S6
S13      36952   1AND12
S14       1342   1AND7
S15       5838   1AND8
S16       1633   1AND9
S17       7685   1AND10
S18      38031   1AND11
S19         47   13AND14AND15
S20         14   13AND14AND15AND16
S21         31   13AND14AND15AND17
S22         35   13AND14AND16AND17
S23         69   13AND15AND16AND17
S24         81   14AND15AND16AND17
S25        339   1AND2AND9
S26        487   S19:S25
S27        196   S26 AND COMPAR?????????/TI,AB,CM
S28        108   S26 AND COMPARE?????????/TI,AB,CM
S29        158   S26 AND COMPARI?????????/TI,AB,CM
S30        189   S28:S29
S31        184   S26 AND MEASUR?????????/TI,AB,CM
S32         97   30AND31
S33       2749    (ANNEAL???? OR  THERMAL??? OR RTP OR RTA OR RAPID??) (6N)(-
              END OR ENDS OR ENDING OR STOP????? OR TERMINAT??????? OR CEAS-
              ??? OR HALT?????)/TI,AB,CM
S34         97   S1:S19 AND S32
S35          3   33AND34
S36      16881   S13:S34 AND PROCESS??????(3N)CONTROL?????????
S37       4313   S13:S34 AND PROCESS??????(3N)(CONTROL??? OR CONTROLLING)/T-
              I,AB,CM
S38      16881   S36:S37
S39      16881   S13:S34 AND S38
S40       1163   S39 AND S8
S41       5312   S39 AND CHAMBER??
S42       1759   S40:S41 AND COMPAR???????(8N)MEASUR???????
S43       1569   S40:S41 AND COMPAR???????(8N)VALUE? ?
S44       2261   S40:S41 AND VALUE? ?(8N)MEASUR???????
S45        757   42AND43AND44
S46         46   (S19:S32 OR S34) AND S45
S47         45   S46 NOT S35
S48      75073   IC=H01L?
```

S49	23	S47 AND S48
S50	10	S47 AND MEASUR?????????/TI,AB
S51	1	S47 AND COMPAR?????????/TI,AB
S52	1	S47 AND COMPARE?????????/TI,AB
S53	1	S47 AND COMPARI?????????/TI,AB
S54	5	S49 AND S50
S55	5	S51:S54
S56	397	S33 AND S1
S57	189	S33 AND S2
S58	64	56AND57
S59	61	S58 NOT (S35 OR S55)
S60	54	S59 AND RANGE??
S61	0	S59:S60 AND (RTA OR RTP)/TI,AB,CM
S62	0	S59:S60 AND (RTA OR RTP)
S63	7	S59:S60 AND ANNEAL???????
S64	16	S59:S60 AND RAPID???(3N)(THERMAL?????? OR HEAT?????? OR TR-EAT??????)
S65	16	S59:S60 AND (THERMAL?????? OR HEAT??????)(3N)TREAT??????
S66	29	S63:S65
S67	1	S66 AND (COMPARE????????? OR COMPARI?????????)/TI,AB
S68	0	S66 AND (VALUE? ?)/TI,AB
S69	4	S66 AND (FEEDBACK????? OR (FED OR FEED????)()BACK)/TI,AB,CM
S70	18	S66 AND (MEASUR?????????)/TI,AB,CM
S71	15	S66 AND (RANG????????)/TI,AB,CM
S72	9	70AND71
S73	12	S67:S69 OR S72
S74	3	S59 AND IC=H01L?
S75	3	S74 NOT S73
S76	23306	1AND2
S77	572	S76 AND IC=H01L?
S78	229	S77 AND (COMPARE??????? OR COMPARI????????)(9N)MEASUR?????-????
S79	188	S77 AND (COMPARE??????? OR COMPARI????????)(9N)(MEASURED??-??????? OR MEASURING)
S80	120	S78:S79 AND (VALUE? ? OR VARIABLE? ? OR PARAMETER? ? OR CO-NDITION? ? OR TEMPERATURE? ? OR POWER)/TI,AB
S81	15	S75 OR S73
S82	0	33AND80
S83	120	76AND80
S84	120	77AND83
S85	7	S84 AND (RTA OR RTP)
S86	16	S84 AND (RAPID??(2N)THERMAL??)
S87	7	S84 AND (RAPID??(2N)HEAT??????)
S88	34	S84 AND (ANNEAL?????? OR (THERMAL?? OR HEAT????)(2N)TREAT?-???)
S89	15	S73:S74
S90	39	S85:S88 NOT S89
S91	30	S90 AND TEMPERATURE? ?(4N)(CHAMBER?? OR VESSEL?? OR CHIP? ? OR SUBSTRATE? ? OR MICROCHIP? ? OR WAFER? ?)
S92	0	90AND33
S93	64	1AND2AND33
S94	49	S93 NOT S89
S95	29	S90:S91 AND TRANSFER?????????
S96	48	S94:S95 AND (COMPARI??????? OR COMPARE????????)(8N)MEASUR?-???????????
S97	31	S96 AND (SEMICOND???????/TI,AB,CM OR S48)
S98	4	77AND33
S99	1	S98 NOT (S89 OR S97)

32/9/1 (Item 1 from file: 350)
DIALOG(R) **File** 350:Derwent WPIX

016190180 **Image available**
WPI Acc No: 2004-348066/**200432**
XRPX Acc No: N04-278538
Semiconductor device e.g. transistor fabrication process controlling method, involves determining operating recipe parameter based on **comparison of measured electrical performance characteristics to its target value**
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI); CHONG R J (CHON-I); WANG J (WANG-I)
Inventor: CHONG R J; WANG J

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200432224	**A1**	**20040415**	**WO 2003US29037**	**A**	**20030919**	**200432**	**B**
US 20040093110	**A1**	**20040513**	**US 2002262620**	**A**	**20020930**	**200432**	
AU 2003270675	**A1**	**20040423**	**AU 2003270675**	**A**	**20030919**	**200465**	

Priority Applications (No Type Date): US 2002262620 A 20020930

Abstract (Basic): **WO 200432224** A1

NOVELTY - The method involves performing a process to form a feature of a semiconductor device based on operating recipe. An electrical performance characteristic of the feature is **measured** and **compared to the target value** for the electrical performance characteristics. A parameter of the operating recipe is determined based on the **comparison. An offset to a base value of a recipe parameter is determined based on the comparison.**

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a semiconductor device manufacturing system.

USE - Used for controlling fabrication process of a semiconductor device e.g. transistor that is utilized in integrated circuit device e.g. microprocessor, digital signal processor, application specific integrated circuit, and memory device.

ADVANTAGE - The method provides reliable semiconductor device meeting its target electrical performance characteristics.

DESCRIPTION OF DRAWING(S) - The drawing shows a block diagram of a portion of a manufacturing system.

Electrical parameter controller (140)
Etch tool (200)
Deposition tool (210)
Plating tool (220)
Polishing tool (230)
Wafers (240)

27/9/1
DIALOG(R) File 2:INSPEC

7915488 INSPEC Abstract Number: B2004-05-0170S-003
Title: In-situ optical wafer temperature measurement
Author(s): Adams, B.; Schietinger, C.
Author Affiliation: Appl. Mater., Santa Clara, CA, USA
Journal: AIP Conference Proceedings Conference **Title**: AIP Conf. Proc. (USA) no.684, pt.2 p.1081-6
Publisher: AIP,
Publication Date: 2003 Country of Publication: USA
CODEN: APCPCS ISSN: 0094-243X
SICI: 0094-243X(2003)684:2L.1081:SOWT;1-S
Material Identity Number: A210-2003-050
U.S. Copyright Clearance Center Code: 0094-243X/03/$20.00
Conference **Title**: Temperature: Its Measurement and Control in Science and Industry. Eighth International Temperature Symposium
Conference Sponsor: Instrumentation, Systems and Automation Soc.; Nat. Institute of Standards and Technol
Conference Date: 21-24 Oct. 2002 Conference Location: Chichago, IL,
Language: English Document Type: Conference Paper (PA); Journal Paper
Treatment: Applications (A)
Abstract: The need for increasingly tighter process control is eminently apparent as **semiconductor** device dimensions become smaller and **wafers** larger. Today "Thermal Budgets" are shrinking and ramp rates are increasing throughout **wafer** processing. **Wafer** temperature is perhaps the most universally critical process variable in front-**end** integrated circuits (IC) manufacturing. The use of **pyrometry** and optical lightpipes continues to gain widespread acceptance as the standard temperature control method in many processes. Lightpipes are used for controlling temperature in chemical vapor deposition (CVD), rapid thermal processing (**RTP**), epitaxial film growth (EPI) and physical vapor deposition (PVD). Optical thermometry offers numerous advantages over other forms of **wafer** temperature **measurement** . This paper presents the current strengths and limitations in optical **wafer** temperature **measurement**. Many factors continue to drive the **measurement** technology. As IC junctions become shallower, thermal budget concerns drive process temperatures down. Processing time and **ramp rates continue to shorten in particular for implant anneals**. Increasingly, process control requires complete thermal histories of wafers throughout IC manufacturing. These factors and new materials (copper and low- kappa dielectrics) push tool manufactures and **pyrometer** vendors toward lower temperatures while still requiring high sensitivity, and accuracy. The accuracy of most in-situ optical temperature **measurement** continues to be dominated by uncertainty in **wafer** emissivity. Factors that limit accuracy, e.g., from **wafer** to **wafer** and from tool to tool, and advances in the technology are discussed. (23 Refs)
Subfile: B
Descriptors: chemical vapour deposition; integrated circuit manufacture; process **control; pyrometers; rapid thermal processing; temperature control; temperature measurement**

97/TI,PN,PD,AN,AD,IC,AB,AB,K/1 (Item 1 from file: 348)
DIALOG(R) **File** 348:**(c)** European Patent Office. All rts. reserv.
Method and apparatus for plasma etching
PATENT (CC, No, Kind, Date): EP 1096547 A2 010502 (Basic)
EP 1096547 A3 040128
PRIORITY (CC, No, Date): US 430798 991029

ABSTRACT EP 1096547 A2

This invention is directed to a method for plasma etching difficult to etch materials at a high etch rate. The method is particularly useful in plasma etching silicon nitride layers more than five microns thick. The method includes a plasma formed by energy provided from two separate **power** sources and a gaseous mixture that includes only an etchant gas and a sputtering gas. The **power** levels from the separate **power** sources and the ratio between the flow rates of the etchant gas and a sputtering gas can be advantageously adjusted to obtain etch rates of silicon nitride greater than two microns per minute. Additionally, an embodiment of the method of the invention provides a two etch step process which combines a high etch rate process with a low etch rate process to achieve high throughput while minimizing the likelihood of damage to underlying layers. The first etch step of the two-step method provides a high etch rate of about two microns per minute to remove substantially all of a layer to be etched the. In the second step, a low etch rate process having an etch rate below about two microns per minute is used remove any residual material not removed by the first etch step.

...SPECIFICATION

Computer controlled processing system 400 includes a mainframe 405, system controller 500 and auxiliary systems 403. Mainframe 405 is the support structure for central **transfer** chamber 410, processing chambers 200, auxiliary chamber 409 and loadlocks 407 and 405. Mainframe 405 also supports gas panel 222, system power panel 415 and pneumatic supply system 422. Common **transfer** chamber 410 which includes a wafer exchange robot 412 (shown in phantom) adapted to move wafers between loadlocks 405 and 407 and the processing and...

. . . etching, physical sputtering, **rapid thermal anneal** and chemical mechanical polishing of dielectric, semiconductor and conductor layers on workpieces such as, for example, semiconductor wafers.

The process gas control task 562 has program code for controlling process gas composition and flow rates for providing...
...desired pressure in the chamber, and then the steps described above would be carried out. As discussed above, the desired process gas flow rates are **transferred** to the process gas control task 562 as process parameters. Furthermore, the process gas control task 562 includes steps for obtaining the necessary delivery gas...control task 563 operates to measure the pressure in the chamber volume 204 by reading one or more conventional pressure manometers connected to the chamber, **compare the measured value to the target pressure**, obtain PID (proportional, integral, and differential) values from a stored pressure table corresponding to the target pressure, and adjust the throttle valve 262 according...

The pedestal **temperature** control task 567 measures the pedestal temperature by **measuring voltage** output of a thermocouple located in pedestal 216, **compares the measured temperature to the setpoint temperature**, and increases or **decreases current applied to the heating element** 258 or temperature controlled fluid to conduits 259 to obtain the setpoint temperature. The temperature is obtained from the **measured** thermocouple **voltage**, for example, by looking up the corresponding temperature in a stored conversion table, or by calculating the temperature using an appropriate mathematical calculation. Additionally, a...

97/TI,PN,PD,AN,AD,IC,AB,AB,K/3 (Item 3 from file: 348)
DIALOG(R) **File** 348:**(c)** European Patent Office. All rts. reserv.
Post-deposition treatment to enchance properties of Si-O-C low K film
PATENT (CC, No, Kind, Date): EP 1077479 A1 010221 (Basic)
INTERNATIONAL PATENT CLASS: **H01L-021/316**; C23C-016/56

ABSTRACT EP 1077479 A1

A method for providing a dielectric film having enhanced adhesion and stability. The method includes a post deposition treatment that densifies the film in a reducing atmosphere to enhance stability if the film is to be cured ex-situ. The densification generally takes place in a reducing environment while heating the substrate. The densification treatment is particularly suitable for silicon-oxygen-carbon low dielectric constant films that have been deposited at low **temperature**.

INTERNATIONAL PATENT CLASS: **H01L-021/316...**

...ABSTRACT environment while heating the substrate. The densification treatment is particularly suitable for silicon-oxygen-carbon low dielectric constant films that have been deposited at low **temperature**.

...SPECIFICATION
. . . deposited from a process gas of ozone and an organosilane precursor having at least one silicon-carbon (Si-C) bond. During the deposition process, the **substrate** is heated to a **temperature** less than about 250(degree)C. In some embodiments, the organosilane precursor has a formula of Si(CH3)))x))H4-x)) where x is either... formation of a carbon-doped silicon oxide layer according to one embodiment of the method of the present invention;

Fig. 4 is a graph of **substrate temperature** versus dielectric constant for a carbon-doped silicon oxide film deposited in accordance with a particular embodiment of the present invention; manager subroutine 77a.

The process control subroutine 85 operates to measure the pressure in the chamber 15 by reading one or more conventional pressure manometers connected to the chamber, to **compare the measure value(s) to the target pressure**, to obtain PID (proportional, integral, and differential) values from a stored pressure table corresponding to the target pressure, and...

...subroutine 87 is also invoked by the chamber manager subroutine 77a and receives a target, or set-point, temperature parameter. The heater control subroutine 87 **measures the temperature by measuring voltage output of a thermocouple located in pedestal 12 chamber 15, or lid assembly 15a, comparing the measured temperature to the set-point temperature, and increasing or decreasing current applied to the heating unit to obtain the set-point temperature.**

The temperature is obtained from the measured voltage by looking up the corresponding temperature in a stored conversion table, or by calculating the temperature using a fourth-order polynomial. When, for example, an...Fig. 3, the film is deposited by flowing an organosilane precursor gas and ozone into a substrate processing chamber and **heating the substrate within the chamber to a temperature less than about 250(degree)C** (step 305).

The present inventors have found that the dielectric constant of carbon-doped silicon oxide film deposited in step 305 is directly related to the **temperature** of the **substrate** during deposition.

As used herein "deposition temperature" refers to the **temperature** of the **substrate** during deposition. In the currently preferred embodiments, the substrate is directly heated by the pedestal heater. At higher pressures, e.g., 200 Torr and above, the **substrate temperature** is practically equal to the pedestal **temperature** (**substrate temperature** may be about 10(degree)C less) due to conduction and convection heating. At near vacuum pressures, however, (e.g., less than 50 Torr) there may be a 50-60(degree)C **temperature** difference between the **substrate** and pedestal because of the lack of convection heating. Thus, at these lower pressure levels, the pedestal temperature can be set up to 50-60...

...CLAIMS reducing atmosphere comprises ammonia (NH3))) at a pressure of between 200 and 700 torr during said densification.

5. The method of claim 4 wherein the **substrate** is heated to a **temperature of between 300 and 500(degree)C** during said densification.

6. The method of claim 5 wherein the substrate is heated for between 1 and...

...of any of the above claims, wherein the curing is done in a furnace.

8. The method of claim 7 wherein said curing heats the **substrate** to a **temperature between 300 and 500(degree)C for at least 15 minutes**.

11. The method of claim 1 wherein said process gas further comprises ozone.

12. The method of claim 1 wherein said **substrate** is heated to a **temperature** of less than about 250(degree)C.

33/9/1
DIALOG(R) **File** 2:INSPEC

7178033 INSPEC Abstract Number: A2002-06-4262A-023, B2002-03-4360B-079
Title: Two-beam laser heating and melting of GaAs crystal layers
Author(s): Zhvavyi, S.P.; Ivlev, G.D.; Gatskevich, E.I.; Sadovskaya, O.L.
Author Affiliation: Inst. of Electron., Nat. Acad. of Sci. of Belarus, Minsk, Belarus
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference **Title**: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.4157 p.200-3
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 2001 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(2001)4157L.200:BLHM;1-W
Material Identity Number: C574-2001-119
U.S. Copyright Clearance Center Code: 0277-786X/01/$15.00
Conference **Title**: Laser-Assisted Microtechnology 2000
Conference Sponsor: SPIE; Ministr. Educ. Russian Federation; Russian Acad. Sci.; Russian Basic Res. Found.; et al
Conference Date: 23-25 Aug. 2000 Conference Location: St. Petersburg-Pushkin, Russia
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Practical (P); Experimental (X)
Abstract: Liquid-solid phase transitions induced in monocrystalline GaAs by two laser beam irradiation have been studied by numerical modeling. The modeling was carried out on the basis of solving the Stefan problem in 1D approximation by a finite difference method. Two variants of combined irradiation by Q-switched ruby and CW Nd:YAG lasers were considered. In the first variant nanosecond radiation from a ruby laser induced the surface melting of a GaAs **wafer** and 'switches on' the absorption of additional CW intensive radiation directed from the back side of the **wafer** through its volume. Two laser beams are directed from one side in the second variant of combined irradiation. As it follows from the data obtained, the motion of the liquid-solid interface can be controlled by changing the intensity of CW radiation. **Because of strong temperature dependence of optical absorption** in solid GaAs at lambda = 1064 nm, a heat wave moving toward Nd:YAG laser radiation can arise near the liquid-solid interface in opposite geometry and screen the melt from the CW laser beam. In the case of one-sided geometry the time dependence of melting depth has a nonmonotone character; **the crystallization process can be terminated and the melting develops again**. (11 Refs)
Subfile: A B
Descriptors: crystallisation; gallium arsenide; III-V semiconductors; laser beam **annealing**; laser beam effects; laser materials processing; melting

37/9/2
DIALOG(R) **File** 2:INSPEC

6752356 INSPEC Abstract Number: A2000-24-8140G-001
Title: Apparatus for real-time observations of the annealing process of metallic glasses
Author(s): Todorow, B.; Bogen, O.v.; Kanellis, S.
Author Affiliation: Dept. of Math., Phys. & Comput. Sci., Ryerson Polytech. Univ., Toronto, Ont., Canada
Journal: Journal of Magnetism and Magnetic Materials Conference **Title**: J. Magn. Magn. Mater. (Netherlands) vol.215-216 p.499-502
Publisher: Elsevier,
Publication Date: June 2000 Country of Publication: Netherlands
CODEN: JMMMDC ISSN: 0304-8853
SICI: 0304-8853(200006)215/216L.499:ARTO;1-M
Material Identity Number: J271-2000-015
U.S. Copyright Clearance Center Code: 0304-8853/2000/$20.00
Conference **Title**: 14th International Symposium on Soft Magnetic Materials(SMM14)
Conference Date: 8-10 Sept. 1999 Conference Location: Balatonfured,Hungary
Document Number: S0304-8853(00)00203-1
Language: **English** Document Type: Conference Paper (PA); Journal Paper(JP)
Treatment: Experimental (X)
Abstract: An apparatus design is proposed for continuous monitoring of the annealing process in metallic glasses based on Joule heating. This provides the opportunity to observe the dynamics of the process, **determine the annealing temperature from the drop in resistivity and to control physical properties by terminating the annealing process at any point** or varying the heating rate and therefore the grain size.

Descriptors: annealing; boron alloys; cobalt alloys; electrical resistivity; grain size; iron alloys; metallic glasses; resistance heating; soft magnetic materials

4/9/1 (Item 1 from file: 34)
DIALOG(R) **File** 34:SciSearch(R) Cited Ref Sci

09018337 Genuine Article#: 356YY Number of References: 122
Title: Automatic control in microelectronics manufacturing: Practices, challenges, and possibilities
Author(s): Edgar TF (REPRINT) ; Butler SW; Campbell WJ; Pfeiffer C; Bode C;
Hwang SB; Balakrishnan KS; Hahn J
Corporate Source: UNIV TEXAS,DEPT CHEM ENGN/AUSTIN//TX/78712 (REPRINT);
TEXAS INSTRUMENTS INC,/DALLAS//TX/; ADV MICRO DEVICES INC,/AUSTIN//TX/;
MOTOROLA INC,/AUSTIN//TX/; HYUNDAI,/INCHON//SOUTH KOREA/
Journal: AUTOMATICA, **2000**, V36, N11 (NOV), P1567-1603
ISSN: 0005-1098 **Publication Date**: 20001100
Publisher: PERGAMON-ELSEVIER SCIENCE LTD, THE BOULEVARD, LANGFORD LANE,
KIDLINGTON, OXFORD OX5 1GB, ENGLAND
Language: English Document Type: REVIEW
Geographic Location: USA; SOUTH KOREA
Subfile: CC ENGI--Current Contents, Engineering, Computing & Technology
Journal Subject Category: ROBOTICS & AUTOMATIC CONTROL; ENGINEERING,
ELECTRICAL & ELECTRONIC
Abstract: Advances in modeling and control will be required to meet future technical challenges in microelectronics manufacturing. The implementation of closed-loop control on key unit operations has been limited due to a dearth of suitable in situ measurements, variations in process equipment and wafer properties, limited process understanding, non-automated operational practices, and lack of trained personnel. This paper reviews the state-of-the-art for process control in semiconductor processing, and covers the key unit operations of lithography, plasma etching, thin film deposition, **rapid thermal processing**, and chemical-mechanical planarization. The relationship of process (equipment) models to control strategies is elaborated because recently there has been a considerable level of activity in model development in industry and academia. A proposed control framework for integrating factory control and equipment scheduling, supervisory control, feedback control, statistical process control, and fault detection/diagnosis in microelectronics manufacturing is presented and discussed. (C) 2000 Elsevier Science Ltd. All rights reserved.
Cited References:
BARNA G, 1994, V7, P115, IEEE T SEMICONDUCTOR

18/9/18 (Item 16 from file: 8)
DIALOG(R) **File** 8:Ei Compendex(R)

05839733 E.I. No: EIP01256551133
Title: Formation of flat monolayer-step-free (110) GaAs surfaces by growth **interruption** **annealing** during cleaved-edge epitaxial overgrowth
Author: Yoshita, M.; Akiyama, H.; Pfeiffer, L.N.; West, K.W.
Corporate Source: Institute for Solid State Physics University of Tokyo, Kashiwa, Chiba 277-8581, Japan
Source: Japanese Journal of Applied Physics, Part 2: Letters v 40 n 3 B Mar 15 2001. p L252-L254
Publication Year: 2001
CODEN: JAPLD8 ISSN: 0021-4922
Language: English
Document Type: JA; (Journal Article) Treatment: X; (Experimental)
Journal Announcement: 0106W5
Abstract: We have characterized, by means of atomic force microscopy, the as-grown and subsequently in situ annealed surfaces of 5 nm GaAs layers grown by molecular beam epitaxy (MBE) on a vacuum-cleaved (110) GaAs surface, and find that a high temperature growth **interruption** and **anneal** remarkably improves the surface morphology of the (110) GaAs layer. **Interruption** of the 490 degree C epitaxial GaAs growth by a 10 minute anneal at 600 degree C under an As//4 overpressure produces an atomically-flat surface free of monolayer step edges over areas measuring several tens of mum on a side. These results suggest that the (110) GaAs surface has much higher stability tinder annealing conditions than under MBE growth conditions. 16 Refs.
Descriptors: **Semiconducting** gallium arsenide; Monolayers; Epitaxial growth; Annealing; Molecular beam epitaxy; Vacuum applications; Pressure effects; Atomic force microscopy

27/9/4
DIALOG(R) File 2:INSPEC

6791269 INSPEC Abstract Number: A2001-03-0720H-001, B2001-02-8540C-002
Title: Design of single-wafer furnace and its rapid thermal processing applications
Author(s): Woo Sik Yoo; Fukada, T.; Kuribayashi, H.; Kitayama, H.; Takahashi, N.; Enjoji, K.; Sunohara, K.
Author Affiliation: WaferMasters Inc., San Jose, CA, USA
Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers, Short Notes & Review Papers) vol.39, no.11 p.6143-51
Publisher: Japan Soc. Appl. Phys,
Publication Date: Nov. 2000 Country of Publication: Japan
CODEN: JAPNDE ISSN: 0021-4922
SICI: 0021-4922(200011)39:11L.6143:DSWF;1-U
Material Identity Number: F221-2000-020
Language: English Document Type: Journal Paper (JP)
Treatment: Applications (A); Practical (P); Experimental (X)
Abstract: A resistively heated, vacuum- and atmospheric-pressure-compatible, single-**wafer** furnace (SWF) system is designed to improve the operational flexibility of conventional furnaces and the productivity of single-**wafer** rapid thermal processing (**RTP**) systems. The heat source design and system operation concepts are described. The temperature **measurement /control** techniques and thermal characteristics of the heat source are described. The heat transfer mechanism between the heat source and Si **wafer** is discussed. Temperature and process uniformity in SWF were demonstrated in TiSi formation, implant **annealing** and thin-oxide formation. The defect-generation phenomenon in Si **wafers** during atmospheric pressure **RTP** in a SWF system is investigated as a function of temperature, process time, **wafer** handling method and speed. Highly repeatable slip-free **RTP** results were achieved in 200-mm-diameter Si **wafers** processed at 1100 degrees C for 60 s (up to 5 times) through the **optimization of the wafer handling method and speed.** (11 Refs)
Descriptors: elemental **semiconductors**; ion implantation; oxidation; **rapid thermal annealing; rapid thermal** processing; resistance furnaces; silicon; **temperature control; temperature measurement; titanium compounds**

97/TI,PN,PD,AN,AD,IC,AB,AB,K/5 (Item 5 from file: 348)
DIALOG(R) **File** 348:**(c)** European Patent Office. All rts. reserv.
Surface treatment of C-doped SiO2 film to enhance film stability during O2 ashing
PATENT (CC, No, Kind, Date): EP 1077477 A1 010221 (Basic)
APPLICATION (CC, No, Date): EP 99402072 990817;
ABSTRACT EP 1077477 A1

A method for forming an insulation layer over a substrate. The method forms a carbon-doped silicon oxide layer by thermal chemical vapor deposition using an organosilane. The carbon-doped silicon oxide layer is subsequently cured and densified. In one embodiment, the cured film is densified in a nitrogen-containing plasma. The method is particularly suitable for deposition of low dielectric constant films, i.e., where k is less than or equal to 3.0. Low-k, carbon-doped silicon oxide methylsilane or di-, tri-, tetra-, or phenylmethylsilane. and ozone. The above method can be carried out in a substrate processing system having a process chamber; a substrate holder, a heater, a gas delivery system, and a **power** supply, all of which are coupled to a controller. The controller contains a memory having a computer-readable medium with a program embodied for directing operation of the system in accordance with above method.

...subroutine 87 is also invoked by the chamber manager subroutine 77a and receives a target, or set-point, temperature parameter. The heater control subroutine 87 **measures** the **temperature** by **measuring voltage** output of a thermocouple located in pedestal 12 chamber 15, or lid assembly 15a, **comparing** the **measured temperature** to the **set-point** temperature, and increasing or decreasing current applied to the heating unit to obtain the set-point temperature. The temperature is obtained from the **measured voltage** by looking up the corresponding temperature in a stored conversion table, or by calculating the temperature using a fourth-order polynomial. When, for example, an...Fig. 3, the film is deposited by flowing an organosilane precursor gas and ozone into a substrate processing chamber and heating the substrate within the **chamber** to a **temperature** less than about 250(degree)C (step 305). The deposition process is a thermal, as opposed to plasma, CVD process. After the film is deposited...

As used herein "deposition temperature" refers to the **temperature** of the **substrate** during deposition. In the currently preferred embodiments, the substrate is directly heated by the pedestal heater. At higher pressures, e.g., 200 Torr and above, the **substrate temperature** is practically equal to the pedestal **temperature** (**substrate temperature** may be about 10(degree)C less) due to conduction and convection heating. At near vacuum pressures, however, (e.g., less than 50 Torr) there may be a 50-60(degree)C **temperature** difference between the **substrate** and pedestal because of the lack of convection heating. Thus, at these lower pressure levels, the pedestal temperature can be set up to 50-60...

...Vias 1624 and gaps 1626 are then filled with a second bulk copper layer 1628 as shown in fig. 16h. The resulting structure is then **annealed** and planarized.

...CLAIMS disposed in a substrate processing chamber, the method comprising:
flowing a process gas comprising ozone and an organosilane into the substrate processing chamber;
heating the **substrate** to a **temperature** of less than about 250(degree)C to form a carbon-doped silicon oxide layer over the substrate;
curing the carbon-doped silicon oxide layer...

...or equal to 3.0.

12. The method of claim 1 wherein densifying includes heating the substrate.
13. The method of claim 12 wherein the **substrate** is heated to a **temperature** of between approximately 350(degree)C and 450(degree)C.

97/TI,PN,PD,AN,AD,IC,AB,AB,K/4 (Item 4 from file: 348)
DIALOG(R) File 348:**(c)** European Patent Office. All rts. reserv.
Lid cooling mechanism and method for optimized deposition of low-k dielectric using tri methylsilane-ozone based processes
PATENT (CC, No, Kind, Date): EP 1077274 A1 010221 (Basic)
APPLICATION (CC, No, Date): EP 99402073 990817;
ABSTRACT EP 1077274 A1

An apparatus and method for depositing thin films. The apparatus generally comprises a process chamber having one or more walls and a lid and two heat exchangers. A first heat exchanger is coupled to the walls and a second heat exchanger is coupled to the lid. The two heat exchangers are configured to provide separate **temperature** control of the walls and lid. Separate control of the lid and wall **temperatures** inhibits reaction of the organosilane within the lid while optimizing a reaction within the chamber. The apparatus implements a method, in which a process gas comprising ozone and an organosilane are admitted through the into a processing while a substrate is heated to form a carbon-doped silicon oxide layer over the substrate. During deposition, the lid is kept cooler than the walls.

SPECIFICATION

...subroutine 87 is also invoked by the chamber manager subroutine 77a and receives a target, or set-point, temperature parameter. The heater control subroutine 87 **measures** the **temperature** by **measuring voltage** output of a thermocouple located in pedestal 12 chamber 15, or lid assembly 15a, **comparing** the **measured temperature** to the **set-point** temperature, and increasing or decreasing current applied to the heating unit to obtain the set-point temperature. The temperature is obtained from the **measured voltage** by looking up the corresponding temperature in a stored conversion table, or by calculating the temperature using a fourth-order polynomial. When, for example, an...Fig. 3, the film is deposited by flowing an organosilane precursor gas and ozone into a substrate processing chamber and heating the substrate within the **chamber** to a **temperature** less than about 250(degree)C (step 305). The deposition process is a thermal, as opposed to plasma, CVD process.

...furnace cured at the same time. An ambient atmosphere of nitrogen (N2))) is provided to the furnace at step 1432. The furnace then heats the **substrate** to a **temperature** of about 400(degree)C for a period of about 30 minutes in step 1433.

The flow diagram of Fig 14e shows the details of...C layer in the same chamber as that used in the plasma densification step. Alternatively, the **substrate containing the Si-O-C film may be transferred to a different chamber for capping**. In step 1451, process gas flows and other process conditions are established. Helium is provided at about 1000 sccm and gaps 1626 are then filled with a second bulk copper layer 1628 as shown in fig. 16h. The resulting structure is then **annealed** and planarized.

...CLAIMS gas comprising ozone and an organosilane having at least one silicon-carbon bond into the substrate processing chamber and control said heater to heat the **substrate** holder to a **temperature** of between 100-250(degree)C.

14. A method for forming an insulation layer over a substrate disposed in a substrate processing chamber having one...

...and a lid, the method comprising:

flowing a process gas comprising ozone and an organosilane through said lid into the substrate processing chamber; heating the **substrate** to a **temperature** of less than about 250(degree)C to form a carbon-doped silicon oxide layer over the substrate;

maintaining the walls at a first temperature...

...in the processing chamber in accordance with the following:

flowing a process gas comprising ozone and an organosilane into the substrate processing chamber;

heating the **substrate** to a **temperature** of less than about 250(degree)C to form a carbon-doped silicon oxide layer over the substrate; densifying said carbon-doped silicon oxide layer...

97/TI,PN,PD,AN,AD,IC,AB,AB,K/6 (Item 6 from file: 348)
DIALOG(R) **File** 348:**(c)** European Patent Office. All rts. reserv.

Method for providing pulsed plasma during a portion of a semiconductor wafer process
PATENT (CC, No, Kind, Date): EP 1071120 A2 010124 (Basic)
EP 1071120 A3 010411
PRIORITY (CC, No, Date): US 360883 990723

ABSTRACT EP 1071120 A2
A method for processing a **semiconductor** wafer with a plasma using continuous RF **power** for a first phase of wafer processing and with pulsed RF **power** for a second phase of wafer processing.

...SPECIFICATION however, is applicable to any plasma enhanced semiconductor wafer processing system such as systems that perform plasma enhanced chemical vapor deposition, physical vapor deposition, plasma **annealing**, and the like. In short, the invention would benefit any system that may cause topographically dependent charging of structures upon a semiconductor wafer.

The system...the bias power supply 106.

A process monitor 108 monitors conditions within the process chamber 101. The process monitor 108 can be any sensor for **measuring a condition that is dependent on the process occuring within the chamber 101**.

The control system bus 312 provides for the **transfer** of data and

CLAIMS 1. A method for processing a **semiconductor** wafer, comprising the steps of:
forming a plasma proximate the wafer;
applying continuous RF power to said plasma while processing the wafer with said plasma...

...structures.
16. The method of any one of the proceeding claims, wherein said plasma is a high density plasma.
17. A method for etching a **semiconductor** wafer with a system having a chamber and a RF power source, comprising the steps of:
providing RF power from the RF power source to...

...20, wherein said condition is an optical emission.
22. A computer readable storage medium having program code embodied therein, said program code for controlling a **semiconductor** processing system during a wafer fabrication process, wherein said **semiconductor** processing system includes a chamber and a RF power supply, said program code controlling the **semiconductor** processing system in accordance with the following steps:
applying continuous RF power for a first phase of a process; and
applying pulsed RF power to...

34/TI,PN,PD,AN,AD,IC,AB,AB,K/4 (Item 3 from file: 349)

CVD NANOPOROUS SILICA LOW DIELECTRIC CONSTANT FILMS
DEPOT CHIMIQUE EN PHASE VAPEUR DE FILMS A CONSTANTE DIELECTRIQUE FAIBLE DE SILICE NANOPOREUSE
Patent and Priority Information (Country, Number, Date):
Patent: **WO 200024050** A1 20000427 (WO 0024050)
Application: WO 99US24918 19991021 (PCT/WO US9924918)
Detailed Description

...subroutine 480 is also invoked by the chamber manager subroutine 440 and receives a target, or set point, temperature parameter. The heater control subroutine 480 **measures** the temperature by **measuring** voltage output of a thermocouple located in a susceptor 12, **compares the measured temperature to the set point temperature**, and increases or **decreases current** applied to the heat module to obtain the set point temperature. The temperature is obtained from the **measured** voltage by looking up the corresponding temperature in a stored conversion table, or by calculating the temperature using a fourth order polynomial.

22 The method of claim 21, wherein the first and the second silicon oxide based films comprise dispersed microscopic voids formed by **annealing** the **substrate** using a temperature profile that **gradually rises to a final temperature of at least** . . .

97/TI,PN,PD,AN,AD,IC,AB,AB,K/2 (Item 2 from file: 348)
DIALOG(R) **File** 348:**(c)** European Patent Office. All rts. reserv.
Apparatus and method for surface finishing a silicon film
PATENT (CC, No, Kind, Date): EP 1085562 A2 010321 (Basic)
EP 1085562 A3 040609
PRIORITY (CC, No, Date): US 399443 990917

ABSTRACT EP 1085562 A2
A method of smoothing a silicon surface formed on a substrate. According to the present invention a substrate having a silicon surface is placed into a **chamber** and heated to a **temperature** of between 1000(degree) - 1300(degree)C.
While the substrate is heated to a temperature between 1000(degree) - 1300(degree)C, the silicon surface is exposed to a gas mix comprising H2)) and HCl in the chamber to smooth the silicon surface.

SPECIFICATION

...pressure control subroutine 174 operates to measure the pressure in the chamber 212 by reading one or more conventional pressure nanometers connected to the chamber, **compare the measure value(s) to the target pressure,** obtain PID (proportional, integral, and differential) values from a stored pressure table corresponding to the target pressure, and adjust...

...control subroutine 176 is also invoked by the chamber manager subroutine 170 and receives a target, or setpoint, temperature parameter.
The lamp control subroutine 176 **measures the temperature by measuring voltage output of the temperature measurement devices directed at the susceptor 220 compares the measured temperature to the setpoint temperature,** and increases or **decreases power** applied to the lamps to obtain the setpoint temperature.

...CLAIMS
or silicon alloy surface of a substrate, said method comprising the steps of:
heating a substrate having a silicon or silicon alloy surface in a **chamber** to a **temperature** of between 1000(degree) - 1300(degree)C; and
exposing said first silicon or silicon alloy surface to a first gas comprising HCl in said chamber...

...a silicon or silicon alloy surface formed on a substrate, said method comprising the steps of:
heating a substrate having a silicon surface in a **chamber** to a **temperature** of between 1000(degree) -1300(degree)C;
exposing said silicon or silicon alloy surface to a gas mix comprising H2)) and HCl in said chamber...

...treating a silicon or silicon alloy surface on a substrate, said method comprising the steps of:
heating a substrate having a silicon surface in a **chamber** to a **temperature** of between 1000(degree) -1300(degree)C;
exposing said silicon or silicon alloy surface to a first gas mix comprising HCl and H2)) while heating...
...surface of a silicon or silicon alloy film of a silicon on insulator substrate, said method comprising the steps of:
heating said substrate in a **chamber** to a **temperature** between 1050(degree)C - 1200(degree)C;
exposing said silicon film to a first gas mix comprising HCl and H2)) in said chamber while heating...

...and body therein for directing operation of said substrate processing system, said computer readable program comprising;
instructions for controlling said heat source to heat said **substrate** to a **temperature** of between 1000(degree)-1300(degree)C, and instructions for controlling said gas delivery systems to introduce a process gas including HCl while heating said **substrate** to a **temperature** of between 1000(degree)-1300(degree)C.

12/9/3 (Item 3 from file: 8)
DIALOG(R) **File** 8:Ei Compendex(R)

05409644 E.I. No: EIP99114894717
Title: Terminal iterative learning control with an application to RTPCVD thickness control
Author: Xu, Jian-Xin; Chen, Yangquan; Lee, Tong Heng; Yamamoto, Shigehiko
Corporate Source: Natl Univ of Singapore, Singapore, Singapore
Source: Automatica v 35 n 9 1999. p 1535-1542
Publication Year: 1999
CODEN: ATCAA9 ISSN: 0005-1098
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical)
Journal Announcement: 9912W3
Abstract: A special type of iterative learning control (ILC) problem is considered. Due to the insufficient measurement capability in many real control problems such as Rapid Thermal Processing (RTP), it may happen that only the terminal output tracking error instead of the whole output trajectory tracking error is available. In the RTP chemical vapor deposition (CVD) of wafer fab. industry, the ultimate control objective is **to control the deposition thickness (DT) at the end of the RTP cycle**. The control profile for the next operation cycle has to be updated using the terminal DT tracking error alone. A revised ILC method is proposed to address this terminal output tracking problem. By parameterizing the control profile with a piecewise continuous functional basis, the parameters are updated by a high-order updating scheme. A convergence condition is obtained for a class of uncertain discrete-time time-varying linear systems including the RTPCVD system as the subset. Simulation results for an RTPCVD thickness control problem are presented to demonstrate the effectiveness of the proposed iterative learning scheme. (Author abstract) 15 Refs.
Descriptors: Intelligent control; Learning systems; Chemical vapor deposition; Rapid thermal annealing; Spatial variables control; Asymptotic stability; Discrete time control systems; Linear control systems; **Semiconductor** device manufacture; Computer simulation

12/9/1 (Item 1 from file: 8)
DIALOG(R) File 8:Ei Compendex(R)

05803648 E.I. No: EIP00025064861

Title: Application of rapid thermal processing technology to the manufacture of integrated circuits - an overview

Author: Bratschun, Alan
Corporate Source: SEMATECH, Austin, TX, USA
Source: Journal of Electronic Materials v 28 n 12 Dec 1999. p 1328-1332
Publication Year: 1999
CODEN: JECMA5 ISSN: 0361-5235
Language: English
Document Type: JA; (Journal Article) Treatment: A; (Applications); G; (General Review)
Journal Announcement: 0104W3

Abstract: Like many of the technologies used to process integrated circuits, the road to manufacturing for rapid thermal processing (RTP) has been twisted. What began as a speculative laboratory apparatus has evolved into a cornerstone of IC technology. Qualities that make RTP desirable for IC manufacture include the ability to process wafers individually, the ability to minimize the time wafers spend at elevated temperature, the convenience of clustering RTP to other systems, and the possibility of maintaining cold reactor walls. This paper will review how these properties make RTP desirable. The paper also will present an overview of the difficulties surrounding the use of RTP and describe how many serious hurdles have been overcome. It will summarize the evolution of RTP from a curiosity to a mainstay technology in building integrated circuits. It then will describe SEMATECH's role in working with RTP, ending with a direction for future application of RTP based on the National Technology Roadmap for Semiconductors (NTRS). (Author abstract) 13 Refs.

Descriptors: *Integrated circuit manufacture; Heat treatment; Ion implantation; Technology transfer

6301774 INSPEC Abstract Number: B1999-09-0170S-001, C1999-09-3350E-001

Title: Using automatic fault detection to improve diffusion furnace performance and reduce wafer scrap

Author(s): Yelverton, M.; Cusson, B.; Timmons, T.; Stoddard, K.
Author Affiliation: AMD, Austin, TX, USA
Journal: Micro vol.17, no.4 p.27-33
Publisher: Canon Communications,
Publication Date: April 1999 Country of Publication: USA
CODEN: MICRFI ISSN: 1081-0595
SICI: 1081-0595(199904)17:4L.27:UAFD;1-W
Material Identity Number: D303-1999-004
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P); Experimental (X)
Abstract: Increased demands on semiconductor manufacturing are driving the development and implementation of advanced control strategies. Partnerships between equipment suppliers and semiconductor manufacturers make these improvements possible through the development of open hardware platforms and data management solutions. Adding sensors to tools where needed and generating sensor data are critical, regardless of whether model-based, run-to-run, or automatic fault detection (AFD) control strategies are implemented. Accurate, reliable in situ information is the foundation on which all control systems should be built. AFD strategies are useful for monitoring and reducing sensor drift and noise, enabling corrective action to be taken before process- and wafer-state variables are affected. This article describes the AFD method of in situ data management used to monitor equipment-state sensors on diffusion furnaces for enhanced furnace performance and reduced wafer scrap. (5 Refs)

27/9/7
DIALOG(R) **File** 2:INSPEC

6204935 INSPEC Abstract Number: C1999-05-3350E-012
Title: Temperature control of rapid thermal processing system using adaptive fuzzy network
Author(s): Chin-Teng Lin; Chia-Feng Juang; Jui-Cheng Huang
Author Affiliation: Dept. of Control Eng., Nat. Chiao Tung Univ., Hsinchu, Taiwan
Journal: Fuzzy Sets and Systems vol.103, no.1 p.49-65
Publisher: Elsevier,
Publication Date: 1 April 1999 Country of Publication: Netherlands
CODEN: FSSYD8 ISSN: 0165-0114
SICI: 0165-0114(19990401)103:1L.49:TCRT;1-Z
Material Identity Number: F061-1999-006
U.S. Copyright Clearance Center Code: 0165-0114/99/$20.00
Document Number: S0165-0114(97)00178-4
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P); Theoretical (T)
Abstract: Temperature control of a rapid thermal processing (**RTP**) system using a proposed self-constructing adaptive fuzzy inference network (SCAFIN) is presented. First, the physical modeling of a **RTP** system is done. An integrated model is given for the components that make up a **RTP** system. The models for the components are integrated in a numerical code to give a computer simulation of the complete RTP system. Then a direct inverse control scheme using the proposed SCAFIN is adopted to control the temperature of the **RTP** system. The SCAFIN is inherently a modified TSK-type fuzzy rule-based model possessing neural network's learning ability. There are no rules initially in the SCAFIN. They are created and adapted as online learning proceeds via simultaneous structure and parameter identification. Simulation results show that the control approach is able to track a temporally varying temperature trajectory and maintain the uniformity of the spatial temperature distribution of the **wafer** in the **RTP** system simultaneously. (19 Refs)
Descriptors: adaptive **control; fuzzy control; fuzzy neural nets; parameter estimation;** process **control; rapid thermal processing; semiconductor** device manufacture; simulation; **temperature control**

35/TI,PN,PD,AN,AD,IC,AB,AB,K/2 (Item 2 from file: 349)
DIALOG(R) File 349:(c) WIPO/Univentio. All rts. reserv.

5,745,594

5,962,862

p 1 of 3

DETECTION OF WAFER FRAGMENTS IN A WAFER PROCESSING APPARATUS

Patent and Priority Information (Country, Number, Date):
Patent: **WO 200022655 A1 20000420 (WO 0022655)**
Application: **WO 99US24382 19991015 (PCT/WO US9924382)**

Main International Patent Class: H01L-021/00

English Abstract

During a rapid thermal process, fragments can break away from a wafer and fall onto a temperature sensor in the process chamber. The wafer fragments can compromise the accuracy of the temperature signals generated by sensor probes. In particular, the fragments can attenuate or otherwise interfere with the radiation received from the wafer. This interference can undermine the accuracy of the temperature measurement signal generated by the probes. If the temperature control function is compromised, excessive temperature gradients can result in damage to the wafer, reducing device yield and degrading device quality. To alleviate the effects of wafer fragments, the presence of a wafer fragment is detected. An image acquisition device acquires an image of a wafer. A processor analyses the acquired image to determine whether a wafer fragment is present. The processor analyzes the acquired image for optical density contrast changes indicative of the presence of a wafer fragment. Detection of a wafer fragment allows the rapid thermal process to be stopped so that the fragment can be cleared away prior to insertion of the next wafer into the deposition process chamber.

Detailed Description

... **be spatially controlled to more effectively minimize thermal gradients across the wafer.**

For spatial control of cross-wafer temperature, particularly with zoned heat sources, a **rapid thermal processing** chamber typically incorporates a **temperature** sensing device. The temperature sensing device may include, for example, an array of temperature sensor probes such as **pyrometers**. The temperature sensing device senses the temperature of the wafer, often at several positions, during the heating cycle.

Temperature signals generated by the **temperature** sensing device are **processed** to generate control signals for the heat source.

Accordingly, the accuracy of the temperature signals provided by the temperature sensing device is important for effective control of the heat source, and 5 therefore is a significant factor in device fabrication quality and yield. Any inaccuracies in the **temperature measurement** can undermine the effectiveness of the temperature control function, opening the door for temperature gradients that can damage the wafer being processed.

...particular, the system and method facilitate the detection of wafer fragments in a deposition processing chamber. Such wafer fragments can adversely affect the accuracy of **temperature measurements** within the chamber.

The system and method are particularly useful in controlling the quality of a **rapid thermal process** given the stringent **temperature** requirements of such a **process**. The system and method may find ready application, however, in a variety of wafer processes in which the presence of fragments is a concern, and therefore are not limited to **rapid thermal** processin .

With **pyrometer** probes, for example, wafer fragments can fall onto the reflector plate at positions generally coincident with the probes. The wafer fragments can attenuate or otherwise interfere with the infrared radiation received from the wafer.

This interference can undermine the accuracy of the **temperature measurement** signal generated by the probes, and ultimately degrade the temperature control function across the surface of the wafer. If the temperature control function is ineffective...

...illuminated background provides an indication of the absence of a portion of the wafer, and thus the potential presence of a wafer fragment on the **temperature measurement** device or some surface between the wafer mount and the **temperature measurement** device.

Optical density contrast can be detected by analyzing the optical densities of pixels in the wafer image and comparing the densities to a target density range.

Once a number of neighboring pixels exhibiting the requisite density range are detected, the size of the area defined by the pixels can value corresponding to a fragment size that could be detrimental to the **temperature measurement** function.

By removing the fragment, a potential source of error in the **temperature measurement** generated by the **temperature** sensing device can be eliminated before the next wafer is processed. In this manner, the accuracy of the **temperature measurement** can be maintained, thereby avoiding processing problems with subsequent wafers in the process run. The result is a reduced probability of excessive temperature gradients that...estimated size can be compared to a threshold size indicative of the size of a wafer fragment that potentially could have an effect on the **temperature measurement** and control functions. As an example, the size of a contrast area can be estimated in terms of the number of image pixels exhibiting the...

p. 2

Sensor probes 30 may take the form of **pyrometers** that transduce infrared radiation emitted by wafer 26 into temperature signals. An example of such a **temperature measurement** system is disclosed in United States Patent No. 5,660,472 to Peuse et al., the entire content of which is incorporated herein by reference. Alternatively, chamber 10 could incorporate an infrared camera, discrete thermocouples, thin filin thermocouples, or other temperature sensing devices appropriate for **measurement** of **temperature** across the surface of wafer 26. The use of **pyrometer**-based sensor probes 30 will be described herein.

The temperature signals generated by sensor probes 30 can be fed back to a controller (not shown...

...information sufficient for the temperature control function, particularly for **zoned lamp sources exhibiting a predetermined spatial heating profile** for a given application.

FIG. 10 is a side view of an alternative viewing chamber 134. Viewing chamber 134 conforms substantially out conventional image processing for the analysis of **optical contrast comparison of the actual and reference images**. As a further alternative, processor 38 could take the form of a custom logic circuit arranged to execute a wafer fragment detection process as...

Claim

I . A system for analysis of a **wafer** for the absence of **wafer** fragments, the system comprising:
a viewing chamber;
a **wafer** support member disposed within the chamber;
an illumination source that generates back-illuminating radiation for a **wafer** positioned on the **wafer** support member; and
an image acquisition device oriented to acquire an image representative of at least an edge portion of the **wafer**.

2 The system of claim 1, further comprising a background surface, wherein the illumination source is disposed on a side of the **wafer** opposite the background surface, the system further comprising an illumination shield disposed within the viewing chamber, the illumination shield defining an interior region and an...

...region, and the exterior region is arranged such that the illuminating radiation illuminates a portion of the background surface adjacent the edge portion of the **wafer** to thereby provide back-illuminating radiation for the edge portion of the **wafer**.
3 The system of claim 2, wherein the illumination shield has a substantially conical shape, the illumination shield including a first substantially circular opening having a first diameter and a second substantially circular opening having a second diameter, wherein the second opening is sized larger than the size of the **wafer** supported in the **wafer** support area such that the illuminating radiation generated by the illumination source light source is not directly incident on a top - 23 surface of the **wafer** but is incident on the background surface proximate to the edge portion of the **wafer**.

4 The system of claim 3, wherein the illumination source projects a substantially ring-like pattern of illuminating radiation.

5 The system of claim 4...

...source extending around a periphery of the lens.

7 The system of claim 1, wherein the illumination source is disposed on a side of the **wafer** adjacent the background surface and opposite the image acquisition device.

8 The system of claim 7, wherein the illumination source projects a substantially ring-like pattern of illuminating radiation toward a side of the **wafer** adjacent the background surface.

9 The system of claim 8, wherein the substantially ring-like pattern of illuminating radiation overlaps the edge portion of the **wafer**.

10 The system of claim 1, further comprising a processor that analyzes the acquired image to detect the absence of a portion of the **wafer**, and generates an advisory in the event the absence of a portion of the **wafer** is detected. - 24

11 The system of claim IO, wherein the processor analyzes the acquired image by identifying an optical density contrast change, and determines whether a portion of the **wafer** is absent based on identification of the optical density contrast change.

12 The system of claim I 1, wherein the processor is configured to analyze...

...by identifying a contrast area having an optical density that contrasts with a target range of optical densities, estimating a size of the contrast area, **comparing** the estimated size to a threshold value, and indicating detection of the absence of a portion of the **wafer** in the event the estimated size exceeds the threshold value.

13 The system of claim 1 0, further comprising a controller that **halts** operation of the **rapid thermal** process chamber in response to generation of the advisory by the processor.

14 The system of claim 10, wherein the viewing chamber forms an integral...

...of claim 10, wherein the processor is further configured to analyze the acquired image by identifying a contrast area along the edge portion of the **wafer** having an optical density that contrasts with a range of optical densities exhibited by back-illuminating radiation, estimating the size of the contrast area, **comparing** the estimated size to a threshold value, and indicating detection of the absence of a portion of the **wafer** in the event the estimated surface area exceeds the threshold value.

16 A system for detecting the presence of a **wafer** fragment in a

p. 3 of 3

55/TI,PN,PD,AN,AD,IC,AB,AB,K/1 (Item 1 from file: 348)
DIALOG(R) **File** 348:**(c)** European Patent Office. All rts. reserv.
Process and apparatus for the deposition of dielectric layers
PATENT (CC, No, Kind, Date): EP 1111664 A2 010627 (Basic)
EP 1111664 A3 040609
PRIORITY (CC, No, Date): US 470561 991223

ABSTRACT EP 1111664 A2

A method of depositing a dielectric film on a **substrate.** comprising depositing a **silicon** oxide layer on the **substrate;** and treating the dielectric layer with oxygen. A layer of FSG having a fluorine content of greater than 7 %, as **measured** by peak height ratio, deposited by HDP CVD, is treated with an oxygen plasma. The oxygen treatment stabilizes the film. In an alternative embodiment of the invention a thin (< 1000 A thick) layer of material such as silicon nitride is deposited on a layer of FSG using a low-pressure strike. The low pressure strike can be achieved by establishing flows of the process gases such that the pressure in the **chamber** is between 5 and 100 millitorr, turning on a bias voltage for a period of time sufficient to establish a weak plasma, which may be capacitively coupled. After the weak plasma is established a source voltage is turned on and subsequently the bias voltage is turned off. Silicon nitride layers deposited using the low pressure strike exhibit good uniformity, strong adhesion, and inhibit outgassing from underlying layers.

...SPECIFICATION

In an alternative embodiment, the low dielectric constant film is formed with a layer of FSG between two layers of silicon nitride. Each silicon nitride...

The various versions of the present invention may be embodied as a **program code for controlling a semiconductor wafer processing system.** The program code may be stored in a suitable computer readable storage medium. The program code can be configured to control a deposition apparatus comprising: a deposition chamber, a gas panel coupled to the chamber, a plasma generating system coupled to the chamber, and a controller coupled to the gas panel, the source power supply and the bias power supply. The controller typically contains the computer readable storage...the present invention.

When pressure control subroutine 85 is invoked, the desired, or target, pressure level is received as a parameter from chamber manager subroutine 77a. Pressure control subroutine 85 operates to measure the pressure in chamber 13 by reading one or more conventional pressure manometers connected to the chamber, **compare the measure value(s) to the target pressure,** obtain proportional, integral, and differential (PID) values from a stored pressure table corresponding to the target pressure, and adjust throttle...

...the pressure table. Alternatively, pressure control subroutine 85 may open or close throttle valve 26 to a particular opening size to regulate the pressure in chamber 13 to a desired pressure or pressure range.

Heater control subroutine 87 includes program code for controlling the temperature of substrate 17 and/or the temperature in the chamber 13. There are at least two basic methods of controlling the chamber temperature. The first method relies on characterizing the substrate temperature as it relates to, among other things, the total power delivered by the plasma. The...

...increases the substrate temperature. Decreasing the power level generally decreases the substrate temperature. The first method may also be used to control the temperature of chamber 13.

Alternatively, the **chamber** or substrate **temperature** may he **measured,** with a thermocouple or **pyrometer** for example, and the temperature controlled with a separate temperature control unit. Such a temperature control unit may comprise heater elements, cooling elements or both. Such heating/cooling elements may be coupled to the substrate

support member 18, the **chamber** 13 or both. Some **chambers** include a separate temperature control unit for the dome 14.

When temperature control subroutine 87 is invoked, the desired, or target, pressure level is received as a parameter from **chamber** manager subroutine 77a. **Temperature** control subroutine 87 operates to **measure** the **temperature** of **chamber** 13 and or substrate 17 by reading one or more conventional temperature sensors connected to the **chamber** and/or substrate, **compare the measure value(s) to a target temperature**, obtain proportional, integral, and differential (PID) values from a stored pressure table corresponding to the target pressure, and adjust some combination of source RF generator 31A, bias RF generator 31B and **chamber**/substrate heating/cooling elements, according to the PID values obtained from the pressure table. Alternatively, temperature control subroutine 87 may set source RF generator 31A...

...**power output setting** of RF generators 31A and 31B, and for tuning matching networks 32A and 32B. Plasma control subroutine 90, like the previously described **chamber** component subroutines, is invoked by **chamber** manager subroutine 77a. Those skilled in the art will recognize that where substrate temperature is regulated by control of the plasma, the temperature control subroutine...the present invention in which oxygen treatment enhances the stability of a FSG layer. In this embodiment, the processing is accomplished within a single processing **chamber**, but it is understood that the process could be adapted to a multichamber system, or could be performed in a series of different **chambers** or systems. Similarly, the process parameters described below are for an 8-inch process wafer, but the process could be modified to accommodate other wafers such as 10-inch wafers.

A wafer is loaded onto the substrate support member in the processing chamber (step 402) through a vacuum-lock door, or slit valve, and moved to the desired processing position. A process gas including a silicon source, a fluorine source, and an oxygen source is introduced into the **chamber** and a high density plasma is formed to deposit a layer of FSG (step 404) over the wafer. In a preferred embodiment, the silicon source...

...CLAIMS

20. The method embodied therein, said program code for **controlling** a semiconductor **wafer processing** system, wherein said semiconductor processing system includes a **chamber**, a silicon containing gas source, an oxygen containing gas source, a source power supply, and a bias power supply, said program code **controlling** the semiconductor **processing** system to deposit low dielectric constant film on a **wafer** in the **chamber** in accordance with the following:

depositing a fluorosilicate glass (FSG) layer on the substrate; exposing said FSG layer to an oxygen environment; and thereafter, depositing a silicon nitride layer on said FSG layer.

23. Apparatus for depositing a low dielectric constant film on a substrate, comprising:

a deposition **chamber**; a gas panel coupled to said deposition **chamber**; a plasma generating system coupled to said **chamber**; and

a controller, coupled to said gas panel, said source power supply and said bias power supply, said controller containing a computer readable storage medium...

...a silicon nitride layer on said FSG layer.

24. An apparatus for depositing a low dielectric constant film over a substrate disposed within a deposition **chamber** of said apparatus, comprising means for depositing a first dielectric layer on the substrate; and means for depositing a uniform second dielectric layer, wherein said...

?/7/TI,PN,PD,AN,AD,IC,AB,AB,K/10 (Item 10 from file: 348)

Method and apparatus for processing a semiconductor substrate

PATENT (CC, No, Kind, Date): EP 843348 A2 980520 (Basic)
EP 843348 A3 981007

PRIORITY (CC, No, Date): US 746631 961113

ABSTRACT EP 843348 A2

The present invention provides systems, methods and apparatus for high **temperature** (at least about 500-800(degree)C) processing of **semiconductor** wafers. The systems, methods and apparatus of the present invention allow multiple process steps to be performed in situ in the same chamber to reduce total processing time and to ensure high quality processing for high aspect ratio devices. Performing multiple process steps in the same chamber also increases the control of the process **parameters** and reduces device damage. In particular, the present invention can provide high **temperature** deposition, heating and efficient cleaning for forming dielectric films having thickness uniformity, good gap fill capability, high density, low moisture, and other desired characteristics.

...SPECIFICATION semiconductor material and cause damage such as point defects. These point defects, which may lead to irregular and nonuniform junction depths, may be feed by **annealing** the implanted semiconductor material at high temperatures (greater than about 900(degree)C). **Annealing** the implanted semiconductor material, however, may further increase the junction depth beyond that desired. With an approach like gaseous diffusion, controlling dopant distribution and junction films are deposited at temperatures less than 500(degree)C in a deposition **chamber**, and **subsequently heated at temperatures greater than 500(degree)C in a different chamber, such as an annealing furnace**, to perform the dopant diffusion to form the doped region.

...chamber manager subroutine 157a, receives a desired target/set-point temperature parameter, Tdes)), as an input (step 580). In step 582, heater control subroutine 167 **measures** the **current temperature** of heater 25 by **measuring voltage** output of a thermocouple located in heater 25. The current temperature is denoted T(k), where k is the current time step of heater control...is based on the thermal shock resistance of the heater 25 at various temperatures. Thus, the desired ramp rate may continuously change based on the **current measured temperature** of the heater, or it may be set at a constant based on a minimum rate that is low enough to avoid thermal shock within...

The actual ramp rate T'(k) is calculated from **measured temperature** T(k) over a range of **temperature measurement** samples. In general, T'des))(T(k)) may be any continuous function of temperature in various embodiments. In the specific embodiment, T'des))(T(k)) is set to be a predetermined constant value. The calculated ramp rate T'(k) is determined by sampling (i.e., **measuring**) the **temperature** at a predetermined sample rate (e.g., 10 times in a power update period, 1 second, in the specific embodiment). Then, an average of the 10 samples is calculated and **compared** to the average of the **previous** 10 samples. The difference between the averages of the first 10 **measured temperatures** and the previous 10 **measured temperatures** is then divided by the power update period to obtain an average **measured temperature**. The derivative of the average **measured temperature** is then calculated to arrive at the calculated ramp rate T'(k). The ramp rate error ErrRRate)) may then determined by taking the difference between...

97/TI,PN,PD,AN,AD,IC,AB,AB,K/11 (Item 11 from file: 348)

Method and apparatus for processing a semiconductor substrate
PATENT (CC, No, Kind, Date): EP 843347 A2 980520 (Basic)
EP 843347 A3 981216

PRIORITY (CC, No, Date): US 748883 961113
ABSTRACT EP 843347 A2

The present invention provides systems, methods and apparatus for high **temperature** (at least about 500-800(degree)C) processing of **semiconductor** wafers. The systems, methods and apparatus of the present invention allow multiple process steps to be performed in situ in the same chamber to reduce total processing time and to ensure high quality processing for high aspect ratio devices. Performing multiple process steps in the same chamber also increases the control of the process **parameters** and reduces device damage. In particular, the present invention can provide high **temperature** deposition, heating and efficient cleaning for forming dielectric films having thickness uniformity, good gap fill capability, high density, low moisture, and other desired characteristics.

...chamber manager subroutine 157a, receives a desired target/set-point temperature parameter, Tdes)), as an input (step 580). In step 582, heater control subroutine 167 **measures** the **current temperature** of heater 25 by **measuring voltage** output of a thermocouple located in heater 25. The current temperature is denoted T(k), where k is the current time step of heater control...is based on the thermal shock resistance of the heater 25 at various temperatures. Thus, the desired ramp rate may continuously change based on the **current measured temperature** of the heater, or it may be set at a constant based on a minimum rate that is low enough to avoid thermal shock within...

...USG films deposited at about 550(degree)C, Fig. 27 is a photomicrograph demonstrating the gap fill capability of the deposited USG film after an **anneal** at about 1000(degree)C and a subsequent wet etch processing, in accordance with a specific embodiment of the present invention. Fig. 27 shows a...temperatures of at least about 550(degree)C has the advantage of being less prone to shrinkage that might result in void formation after an **annealing** step and a subsequent wet etch processing, compared to USG films deposited at lower temperatures. The dense nature of the deposited USG film makes it...

...applications. Due to its high density, USG films deposited at high temperatures and used as oxide filling layers can be planarized by either a subsequent **anneal** or a CMP step, with minimized likelihood of opening up voids. In addition to moisture absorption resistance and good film thickness uniformity, the present USG...

...wafer. The lack of a plasma from such treatments in the chamber thus reduces possibility of metal contamination and potential shorting of devices in the **wafer**. Compared to low **temperature** thermal USG films, which often require a plasma densification treatment or plasma oxide cap and may shrink to open voids after an **anneal**, thermal USG films deposited at temperatures of about 550(degree)C exhibit excellent gap fill capability, minimal shrinkage, and uniform film density, and low metal...

55/TI,PN,PD,AN,AD,IC,AB,AB,K/5 (Item 4 from file: 349)
DIALOG(R) **File** 349:(**c**) WIPO/Univentio. All rts. reserv.
TEMPERATURE MEASUREMENT AND HEAT-TREATING METHODS AND SYSTEMS
Patent and Priority Information (Country, Number, Date):
Patent: **WO 200360447 A1 20030724 (WO 0360447)**
Application: **WO 2002CA1987 20021223 (PCT/WO CA0201987)**

English Abstract
Temperature measurement and heat-treating methods and systems. One method includes measuring a present intensity of radiation thermally emitted from a first surface of a workpiece, and identifying a present temperature of the first surface in response to the present intensity and at least one previous thermal property of the first surface. Preferably, the workpiece includes a semiconductor wafer, and the first and second surfaces respectively include device and substrate sides thereof. The present temperature of the device side is preferably identified while the device side is being irradiated, e.g. by an irradiance flash having a duration less than a thermal conduction time of the wafer. The device side temperature may be identified in response to a previous device side temperature, which may be identified in response to a previous temperature of the substrate side unequal to the previous device side temperature, and a temperature history of the wafer.

Detailed Description
... of the system to correct the inconsistencies as they are developing, rather than processing a large number of wafers only to discover that **poor reproducibility control of the thermal processing cycle** has led to detrimental performance differences from wafer to wafer.

"While block 606 and 608 continue to execute, block 610 directs the processor circuit 1 5 110 to **compare the most recently received substrate temperature value to a predefined intermediate temperature at which the flash cycle is to be commenced.**"

BRIEF DESCRIPTION OF THE DRAWINGS
Figure 2 is a block diagram of a **rapid thermal** processing system computer (RSQ, a diagnostic illumination source, an imaging device, and a synchronization module, of ...chart of a hemispherical reflectivity routine executed by the 5 processor circuit shown in Figure 2.
Figure 8 is a flow chart of a substrate **temperature** routine executed by a **processor** circuit of the fast radiometer shown in Figure 3.
Figure 9 is a flow chart of a real-time device side **temperature** routine executed by a **processor** circuit of the ultra-fast radiometer shown in Figure 4.
Figure 10 is a circuit diagram of a flash lamp power control circuit **controlled** by the **processor** circuit shown in Figure 4.
Figure 11 is a circuit diagram of a flash lamp power control circuit **controlled** by the **processor** circuit shown in Figure 4, according to a second embodiment of the invention.
Figure 12 is a circuit diagram of a flash lamp power control circuit **controlled** by the **processor** circuit shown in Figure 4, according to a third embodiment of the invention.
Figure 13 is a perspective view of a system for **temperature measurement** and for heat-treating a workpiece, according to a fourth embodiment of the invention, shown with two vertical front-side walls removed.

DETAILED DESCRIPTION
The standard ratio routine 222 includes various blocks of instruction codes which configure the processor circuit 110...no devices and uniform dopant concentration) may be periodically thermally cycled in the system 100, and resulting dopant activation may be measured (for example, by measuring sheet resistance of the wafer). Alternatively, other factors may suggest a desire for recalculation of RatiOSTD, such as a movement of the image of the wafer, or **drastic changes in temperature measurements in one cycle as compared to previous cycles, for example.**

Temperature Monitoring and Control Routine
The remaining routines employ at least some information derived directly or indirectly from wafer reflectivity ...to an intermediate temperature of 800 'C at a ramp rate of 250 'C/second). When the intermediate temperature is reached, the temperature monitoring and **control** routine directs the **processor** circuit to **control** the irradiance system 180 to initiate a flash cycle, to heat the device side 122 of the wafer 120 to a desired **annealing temperature,** at a rate much faster than the thennal conduction time of the wafer (as a further arbitrary illustrative example, the device side may be exposed... the realtime device side temperature routine 420.

15/9/3
DIALOG(R) **File** 2:INSPEC

6672753 INSPEC Abstract Number: B2000-09-2550-016
Title: Silicide sheet resistivity and metal film stress **measurements** as emissivity-independent **techniques for RTP temperature monitoring**
Author(s): Jonak-Auer, I.
Author Affiliation: Austria Mikro Syst. Int. AG, Unterpremstatten, Austria
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference **Title:** Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.3884 p.316-23
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1999 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1999)3884L.316:SSRM;1-1
Material Identity Number: C574-1999-346
U.S. Copyright Clearance Center Code: 0277-786X/99/$10.00
Conference **Title:** In-Line Methods and Monitors for Process and Yield Improvement
Conference Sponsor: SPIE
Conference Date: 22-23 Sept. 1999 Conference Location: Santa Clara, CA, USA
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Experimental (X)
Abstract: **Transfer** of **semiconductor** process steps from one Rapid Thermal Processing (**RTP**) system to another may cause severe problems due to non-matching **pyrometers** . Resulting temperature differences of alternatively used **RTP** machines despite identical process recipes can lead to process and yield problems. In this study we present two emissivity-independent methods for **comparing** and adjusting **wafer** temperatures of different **RTP** systems, one by monitoring titanium silicide (TiSi/sub x/) sheet resistivities and the other by titanium film stress **measurements** . We perform sheet resistivity **measurements** on various titanium sputtered silicon **wafers**. TiSi/sub x/ formation is induced by **RTP** on an AST SHS 1000 and an AG HEATPULSE 4100 system in the temperature range between 680 degrees C and 800 degrees C, which is of particular interest for **RTP** nitridation of titanium as a diffusion barrier. Prior to resistivity **measurement** the unreacted titanium is selectively etched. We show how temperature differences of the two **RTP** systems can be deduced from different sheet resistivity values of AST and AG **wafers** processed at the same nominal temperatures as read on the respective **pyrometer** scales. Comparison of mechanical stress imposed on the **wafers** by titanium deposition and the subsequent **RTP** induced silicidation yield exactly the same temperature difference. Both methods offer fast, reliable and sensitive tools to observe and correct for potential temperature differences of different **RTP** systems and therefore comprise efficient means to avoid process and yield problems and enhance throughput. (5 Refs)
Subfile: B
Descriptors: electrical resistivity; process monitoring; **rapid thermal processing**; stress **measurement; temperature measurement; thermal stresses**; titanium compounds

7/9/1 (Item 1 from file: 350)
DIALOG(R) **File** 350:Derwent WPIX

016042736 **Image available**
WPI Acc No: 2004-200587/**200419**
XRPX Acc No: N04-159206
Pattern and image **comparison** method for inspecting semiconductor chip, involves determining point-by-point relationship between points defining boundary feature in image and pattern
Patent Assignee: COGNEX CORP (COGN-N)
Inventor: GARAKANI A; TAYCHER L
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6687402	B1	20040203	US 98216048	A	19981218	200419	B
			US 2001761	A	20011023		

Priority Applications (No Type Date): US 98216048 A 19981218; US 2001761 A 20011023
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6687402	B1		19	G06K-009/48	Cont of application US 98216048

Abstract (Basic): **US 6687402** B1

NOVELTY - Point-by-point relationships between points defining boundary feature of image and points in pattern are determined by numerical score falling below/above threshold as function of difference in location, angle, contrast point on boundary feature in image and corresponding point on pattern. Function which defines relationship between boundary feature in image, and pattern is determined from relationships.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for automated image analysis system.

USE - For **comparing** patterns and images of semiconductor chips in automated manufacturing and inspection lines.

ADVANTAGE - Removes images of extraneous portions and noise without limitation, and provides contrast enhancement and windowing.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the automated image analysis system.

image analysis systems (10,20)
object (12)
platform (15)
capturing device (16)
communication path (18)
pp; 19 DwgNo 1/7

Title Terms: PATTERN; IMAGE; **COMPARE**; METHOD; INSPECT; SEMICONDUCTOR; CHIP; DETERMINE; POINT; POINT; RELATED; POINT; DEFINE; BOUNDARY; FEATURE; IMAGE; PATTERN
Derwent Class: T01; U11
International Patent Class (Main): G06K-009/48
File Segment: EPI
Manual Codes (EPI/S-X): T01-G02A1; T01-J10B2; U11-F01B3; U11-F01D3

97/TI,PN,PD,AN,AD,IC,AB,AB,K/8 (Item 8 from file: 348)
DIALOG(R) **File** 348:**(c)** European Patent Office. All rts. reserv.
Intergrated CVD/PVD Al planarization using ultra-thin nucleation layers
PATENT (CC, No, Kind, Date): EP 871218 A2 981014 (Basic)
EP 871218 A3 990707
PRIORITY (CC, No, Date): US 838839 970411

ABSTRACT EP 871218 A2
The present invention provides a method and apparatus for forming an interconnect with application in small feature sizes (such as quarter micron widths) having high aspect ratios. Generally, the present invention provides a method and apparatus for depositing a wetting layer for subsequent physical vapor deposition to fill the interconnect. In one aspect of the invention, the wetting layer is a metal layer deposited using either CVD techniques or electroplating, such as CVD aluminum (Al). The wetting layer is nucleated using an ultra-thin layer, denoted as (epsilon) layer, as a nucleation layer. The (epsilon) layer is preferably comprised of a material such as Ti, TiN, Al, Ti/TiN, Ta, TaN, Cu, a flush of TDMAT or the like. The (epsilon) layer may be deposited using PVD or CVD techniques, preferably PVD techniques to improve film quality and orientation within the feature. Contrary to conventional wisdom, the (epsilon) layer is not continuous to nucleate the growth of the CVD wetting layer thereon. A PVD deposited metal is then deposited on the wetting layer at low **temperature** to fill the interconnect.

...SPECIFICATION

...from about 10 sccm to about 200 sccm. The chamber pressure is preferably maintained at from about 0.2 Torr to about 2 Torr. The **wafer is maintained at a temperature of from about 20(degree)C to about 450(degree)C for about a few seconds up to about two minutes or more** while the...

...to limit the scope of the invention. The apparatus 35 typically comprises a cluster of interconnected process chambers, for example, CVD and PVD deposition and **rapid thermal annealing** chambers.

The apparatus 35 includes at least one enclosed PVD deposition chamber 36 for performing PVD processes, such as sputtering. The PVD chamber 36 comprises the substrate into and out of the chamber 40. A thermal heater 80 is then provided in the chamber to **rapidly heat** the substrate. **Rapid heating** and cooling of the substrate is preferred to increase processing throughput, and to allow rapid cycling between successive processes operated at different **temperatures** within the same **chamber** 65. The **temperature** of the **substrate** is generally estimated from the temperature of the support 65.

...the chamber manager subroutine 144a and receives a ramp rate temperature parameter of at least about 50 (degree)C/min.

The heater control subroutine 148 **measures** temperature by **measuring voltage** output of a thermocouple located in the support, **compares** the **measured temperature** to the **setpoint** temperature, and increases or decreases current applied to the heater 80 to obtain the desired ramp rate or setpoint temperature. **The temperature is obtained from the measured voltage** by looking up the corresponding temperature in a stored conversion table, or by calculating the temperature using a fourth order polynomial. When radiant lamps are...

...indicates that the plasma has not been ignite, and the plasma control subroutine 149 restarts or shuts down the process. **The read power levels are compared against target levels,** and the current is adjusted to control the plasma for applying a sinusoidal wave current to the generator to form a rotating magnetic field 5500A of Al was deposited using 2kW of power and the **wafer temperature** was about 400(degree)C. Electron micrographs show good step coverage and void free via-fill.

97/TI,PN,PD,AN,AD,IC,AB,AB,K/9 (Item 9 from file: 348)
DIALOG(R) File 348:**(c)** European Patent Office. All rts. reserv.
Low **temperature** via and trench fill process by means of CVD of Cu followed by PVD of Cu
PATENT (CC, No, Kind, Date): EP 856884 A2 980805 (Basic)
EP 856884 A3 981014
PRIORITY (CC, No, Date): US 792292 970131

ABSTRACT EP 856884 A2
The disclosure relates to a process for providing complete via a trench fill on a substrate.The planarization of Cu layers forms continuous, void-free contacts or vias in sub-half micrometer applications. A refractory layer (12) is deposited onto a substrate having high aspect ratio contacts or vias (14) formed thereon. A CVD Cu layer (22) is then deposited onto the refractory layer at low temperatures to provide a conformal wetting layer for a PVD Cu. Next, a PVD Cu (23) is deposited onto the previously formed CVD Cu layer at a temperature below that of the melting point temperature of Cu. The resulting CVD/PVD Cu layer is substantially void-free. The metallization process is preferably carried out in an integrated processing system that includes both a PVD and CVD processing chamber so that once the substrate is introduced into a vacuum environment, the metallization of the vias and contacts occurs without the formation of an oxide layer over the CVD Cu layer. The via fill process of the present invention is also successful with air-exposure between the CVD Cu and PVD Cu steps.

...SPECIFICATION
A process sequencer subroutine 143 comprises program code for accepting the identified process chamber and set of process parameters from the process selector subroutine 142...control subroutine 147, heater control subroutine 148, and plasma control subroutine 149. These different subroutines function as seeding program code means for (i) heating the **substrate to temperatures TS)) within a range of temperatures . . .**

...temperatures TS)) within the range of temperatures (DELTA) TS)). Typically, the subroutine 148 is programmed to ramp up the temperature of the support from ambient **chamber temperatures** to a set point **temperature.** When the **substrate** reaches the seeding **temperatures** TS)), the process gas control subroutine 146 is programmed to introduce seeding gas into the chamber, as described above. The heater control subroutine 148 also comprises epitaxial growth heating program code 160 for **rapidly heating** the **substrate** to deposition **temperatures** Td)) within a range of temperatures (DELTA) TD)) that are suitable for growing an epitaxial growth layer on the seeding layer. In this step, the...

...the chamber manager subroutine 144a and receives a ramp rate temperature parameter of at least about 50 (degree)C/min.
The heater control subroutine 148 measures temperature by measuring voltage output of a thermocouple located in the support, compares the measured temperature to the setpoint temperature, and increases or decreases current applied to the heater 80 to obtain the desired ramp rate or setpoint temperature. The temperature is obtained from the measured voltage by looking up the corresponding temperature in a stored conversion table, or by calculating the temperature using a fourth order polynomial. When radiant lamps are...

...indicates that the plasma has not been ignited, and the plasma control subroutine 149 restarts or shuts down the process. **The read power levels are compared against target levels,** and the current is adjusted to control the plasma for applying a sinusoidal wave current to the generator to form a rotating magnetic field...

...CLAIMS method as claimed in any of claims 1 to 7, wherein the physical vapor deposited copper includes tin, the method further comprising the step of **annealing** at a temperature of between about 250 C and about 450 C.
9. A process for filling a via, trench or dual damascene structure on a substrate...

...claimed in any of claims 9 to 15, wherein the CVD and PVD Cu layers integrate to form a single conformal metal layer.

37/9/4
DIALOG(R) **File** 2:INSPEC

5986082 INSPEC Abstract Number: A9818-6865-001
Title: Chemical kinetics of mobile-proton generation and annihilation in SiO/sub 2/ thin films
Author(s): Vanheusden, K.; Warren, W.L.; Fleetwood, D.M.; Schwank, J.R.; Shaneyfelt, M.R.; Draper, B.L.; Winokur, P.S.; Devine, R.A.B.; Archer, L.B. ; Brown, G.A.; Wallace, R.M.
Author Affiliation: US Air Force Res. Lab., Kirtland Air Force Base, NM, USA
Journal: Applied Physics Letters vol.73, no.5 p.674-6
Publisher: AIP,
Publication Date: 3 Aug. 1998 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951
SICI: 0003-6951(19980803)73:5L.674:CKMP;1-0
Material Identity Number: A135-98032
U.S. Copyright Clearance Center Code: 0003-6951/98/73(5)/674(3)/$15.00
Document Number: S0003-6951(98)02830-7
Language: English Document Type: Journal Paper (JP)
Treatment: Experimental (X)
Abstract: The chemical kinetics of mobile-proton reactions in the SiO/sub 2/ film of Si/SiO/sub 2//Si structures were analyzed as a function of forming-gas anneal parameters in the 300-600 degrees C temperature range. Our data show that the initial buildup of mobile protons is limited by the rate of lateral hydrogen diffusion into the SiO/sub 2/ films. The final density of mobile protons is **determined by the cooling rate which terminates the annealing process and, in the case of subsequent anneals, by the temperature of the final anneal**. To explain the observations, we propose a dynamical equilibrium model which assumes a reversible interfacial reaction with a temperature-dependent balance. (14 Refs)
Subfile: A
Descriptors: diffusion; elemental semiconductors; ionic conductivity; semiconductor-insulator-semiconductor structures; silicon; silicon compounds

27/9/8
DIALOG(R) **File** 2:INSPEC

6010755 INSPEC Abstract Number: B9810-2550E-031
Title: Ellipsometry-based process monitoring and control for ultrathin gate dielectrics
Author(s): Massoud, H.Z.
Author Affiliation: Dept. of Electr. & Comput. Eng., Duke Univ., Durham, NC, USA
Conference **Title**: Proceedings of the Symposium on Silicon Nitride and Silicon Dioxide Thin Insulating Films. p.208-16
Editor(s): Deen, M.J.; Brown, W.D.; Sundaram, K.B.; Raider, S.I.
Publisher: Electochem. Soc, Pennington, NJ, USA
Publication Date: 1997 Country of Publication: USA xiii+588 pp.
ISBN: 1 56677 137 4 Material Identity Number: XX98-00730
Conference **Title**: Proceedings of the Symposium on Silicon Nitride and Silicon Dioxide Thin Insulating Films
Conference Date: 4-9 May 1997 Conference Location: Montreal, Que., Canada
Language: English Document Type: Conference Paper (PA)
Treatment: Experimental (X)
Abstract: This paper describes the use of automated in situ real-time high-temperature ellipsometry in the monitoring of the growth of ultrathin dielectrics and its use in the **temperature control of rapid-thermal** processing oxidation equipment. The control process is based on oxide-thickness monitoring while **executing temperature control and ending the oxide growth process** when the desired thickness is reached. Results are presented in the growth of 10 nm thick oxides.
Descriptors: dielectric thin films; ellipsometry; monitoring; oxidation; process **control; rapid thermal processing; temperature control; thickness measurement**
Identifiers: process monitoring; process **control**; ultrathin gate dielectric growth; automated in situ real-time high-temperature ellipsometry; **temperature control; rapid thermal processing oxidation**; thickness monitoring
Class Codes: B2550E (Surface treatment for semiconductor devices); B7320C (Spatial variables measurement); B7320R (Thermal variables measurement)

27/9/9
DIALOG(R) File 2:INSPEC

5953098 INSPEC Abstract Number: B9808-2550-006, C9808-3350E-006
Title: A GUI-based concurrent software tool for thermal modeling and control system design of RTP chambers. II. Thermal model development
Author(s): Ghosal, S.; Ebert, J.L.; Chung, K.; Aral, G.; Emami-Naeini, A.
Author Affiliation: Dept. of Appl. Solutions, Integrated Syst. Inc., Sunnyvale, CA, USA
Conference **Title**: Proceedings of the Second International Symposium on Process Control, Diagnostics, and Modeling in Semiconductor Manufacturing p.126-33
Editor(s): Meyyappan, M.; Economou, D.J.; Butler, S.W.
Publisher: Electrochem. Soc, Pennington, NJ, USA
Publication Date: 1997 Country of Publication: USA ix+347 pp.
ISBN: 1 56677 136 6 Material Identity Number: XX98-00574
Conference **Title**: Proceedings of the Second International Symposium on Process Control, Diagnostics, and Modelling in Semiconductor Manufacturing
Conference Date: 4-9 May 1997 Conference Location: Montreal, Que., Canada
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Theoretical (T)
Abstract: This paper is the second of two papers describing the Virtual Concurrent Design Tool (VCDT), a GUI-based software tool that facilitates integrated design of a **RTP** chamber and the associated temperature control system, and describes the thermal modeling method. The VCDT is implemented within the framework of Integrated Systems' MATRIX/sub x/ product family which includes graphical modeling, simulation, and control design software. The VCDT allows one to perform rapid, yet accurate, dynamic heat transfer simulations suitable for model-based feedback control design. This tool models two-dimensional (axisymmetric) geometries using either the control volume-finite element method, or a purely finite element method for triangular meshes. The radiative exchange factors are calculated using a Monte-Carlo method. The simulations yield transient **temperature profiles for wafer**, window, guard-ring, etc., **during the process cycle. (7 Refs)**
Descriptors: concurrent engineering; **control** system analysis computing; **control** system CAD; design engineering; feedback; finite element analysis; graphical user interfaces; heat radiation; Monte Carlo methods; process **control; rapid thermal processing; semiconductor** process modelling; software tools; **temperature control; thermal analysis**; transient analysis

27/9/13
DIALOG(R) File 2:INSPEC

5647197 INSPEC Abstract Number: A9717-6855-134, B9709-0520-006
Title: In situ monitoring of crystallinity and temperature during rapid thermal crystallization of silicon on glass
Author(s): Subramanian, V.; Degertekin, F.L.; Dankoski, P.; Khuri-Yakub, B.T.; Saraswat, K.C.
Author Affiliation: Dept. of Electr. Eng., Stanford Univ., CA, USA
Journal: Journal of the Electrochemical Society vol.144, no.6 p. 2216-21
Publisher: Electrochem. Soc,
Publication Date: June 1997 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651
SICI: 0013-4651(199706)144:6L.2216:SMCT;1-9
Material Identity Number: J010-97007
U.S. Copyright Clearance Center Code: 0013-4651/97/$7.00
Language: English Document Type: Journal Paper (JP)
Treatment: Applications (A); Experimental (X)
Abstract: A novel technique is presented for simultaneously **measuring temperature** and crystallinity in situ during the rapid thermal **annealing** of thin Si films on transparent substrates for active matrix liquid crystal display applications. This technique makes use of acoustic waves to **monitor temperature by measuring changes in Lamb wave velocity with temperature**. Since this technique is independent of emissivity, it enables accurate tracking of crystalline phase transitions along with temperature, based on changes in the optical absorption properties of the film. This provides a methodology for closed-loop control and **end-point detection**. The experiments on thin amorphous Si on fused silica demonstrate temperature repeatability of 2%. Also, the technique proved sensitive enough to detect the onset of nucleation, as evidenced by transmission electron microscopy. (12 Refs)
Descriptors: acoustic wave velocity; amorphous **semiconductors**; crystal structure; crystallisation; CVD coatings; elemental **semiconductors**; light absorption; nucleation; **rapid thermal annealing**; **semiconductor growth|s**; **semiconductor** thin films; silicon; surface acoustic waves; **temperature measurement**; **transmission electron microscopy**

27/9/15
DIALOG(R) File 2:INSPEC

5620879 INSPEC Abstract Number: B9708-2550-003
Title: Temperature measurement in rapid thermal processing
Author(s): Timans, P.J.
Author Affiliation: AG Associates, San Jose, CA, USA
Journal: Solid State Technology vol.40, no.4 p.63-4, 66, 68, 70, 73-4
Publisher: PennWell Publishing,
Publication Date: April 1997 Country of Publication: USA
CODEN: SSTEAP ISSN: 0038-111X
SICI: 0038-111X(199704)40:4L.63:TMRT;1-J
Material Identity Number: S046-97005
U.S. Copyright Clearance Center Code: 0038-111X/97/$1.00+.35
Language: English Document Type: Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: The stringent process uniformity and repeatability requirements of future **semiconductor** processing demand continuing improvement in **wafer** temperature control during rapid thermal processing (**RTP**). The **wafer** itself is the most important and unpredictable variable in an **RTP** system, as its optical properties dominate its thermal response. Basic heat transfer models, which include the thermal radiative properties of **wafers**, have been used to evaluate several **RTP** temperature **measurement** and control schemes. Simple methods can deliver good repeatability in a production environment by relying on the integration of the **wafer** 's spectral emissivity over a wide waveband. (8 Refs)
Subfile: B
Descriptors: emissivity; **rapid thermal processing**; **semiconductor** technology; spectral methods of temperature **measurement**

27/9/16
DIALOG(R) **File** 2:INSPEC

5490547 INSPEC Abstract Number: B9703-2550-015
Title: Pattern related non-uniformities during rapid thermal processing
Author(s): Bremensdorfer, R.; Marcus, S.; Nenyei, Z.
Author Affiliation: AST Elektron., Tempe, AZ, USA
Conference **Title**: Rapid Thermal and Integrated Processing V. Processing p.327-33
Editor(s): Gelpey, J.C.; Ozturk, M.C.; Thakur, R.P.S.; Fiory, A.T.; Roozeboom, F.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1996 Country of Publication: USA xi+389 pp.
Material Identity Number: XX96-03541
Conference **Title**: Rapid Thermal and Integrated Processing V. Symposium
Conference Date: 8-12 April 1996 Conference Location: San Francisco, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Experimental (X)
Abstract: State of the art rapid thermal processing is able to produce a lateral thermal homogeneity which is within the inherent resolution limits of current metrology. For the most commonly used direct or indirect control methods such as multiple thermocouple **measurements**, rapid thermal oxidation (RTO), or rapid thermal **annealing** (**RTA**) of plain **semiconductor wafers** , this limit is +or-2 degrees C. As homogeneity requirements approach those limits, pattern induced nonuniformities are becoming more important. In order to achieve rapid heating and high substrate temperatures in **RTP**, heater and substrate are not in equilibrium and their emission spectra differ considerably. Under such circumstances, laterally varying optical characteristics on the substrate itself imply thermal nonuniformities. The influence of patterns on a silicon **wafer** surface on the temperature uniformity is studied. Passive patterns showing interference effects were formed from thermal oxide and Si_3N_4. RTO and **RTA** , as well as embedded thermocouples were used for temperature **measurement** . The data presented show that major nonuniformities due to interference effects can be reduced by restricting the energy transfer through the patterned side of the **wafer**. It is shown that independent top and bottom heater bank control and controlled thermal kinetics are suitable methods to reduce pattern related process nonuniformities. (5 Refs)
Subfile: B
Descriptors: emissivity; heating; integrated circuit **measurement**; integrated circuit testing; integrated circuit yield; oxidation; **rapid thermal annealing; rapid thermal** processing; temperature distribution; **temperature measurement; thermocouples**

27/9/17
DIALOG(R) **File** 2:INSPEC

5485033 INSPEC Abstract Number: B9703-2550-010, C9703-3350E-003
Title: **Accurate estimation of radiative and convective losses in a multizone RTP reactor**
Author(s): Nagabushnam, R.V.; Singh, R.K.; Sharan, S.; Sandhu, G.
Author Affiliation: Dept. of Mater. Sci. & Eng., Florida Univ., Gainesville, FL, USA
Conference **Title**: Rapid Thermal and Integrated Processing V. Processing p.95-102
Editor(s): Gelpey, J.C.; Ozturk, M.C.; Thakur, R.P.S.; Fiory, A.T.; Roozeboom, F.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1996 Country of Publication: USA xi+389 pp.
Material Identity Number: XX96-03541
Conference **Title**: Rapid Thermal and Integrated Processing V. Symposium
Conference Date: 8-12 April 1996 Conference Location: San Francisco, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Theoretical (T); Experimental (X)
Abstract: We have developed a methodology aimed at accurately determining the various forms of energy transfer (convective loss, radiative loss and absorption of lamp energy by the **wafer**) occurring in any advanced **RTP** system, based on basic system identification experiments and a simple 3D physical model depicting the heat transfer processes. The identification experiments help in estimating uncertain system dependent factors which characterize the various forms of energy **transfer**, which may be otherwise difficult to calculate on a purely theoretical basis. This methodology forms the basic building block of our effort to develop a tool which can predict the temperature distribution across the **wafer** in a realistic way. This tool can be used both as a **wafer** temperature control algorithm in any advanced **RTP** system by incorporating more accurate system impedance parameters (convective and radiative loss) as well as by an **end** user to calculate the required power level settings to various lamp zones to attain reasonable temperature uniformity for a **RTP** system which does not have a dynamic control. (13 Refs)
Subfile: B C
Descriptors: convection; heat losses; heat radiation; identification; integrated circuit testing; process **control**; **rapid thermal processing**; **semiconductor** process modelling; **temperature control**; **temperature distribution**; thermal analysis

97/TI,PN,PD,AN,AD,IC,AB,AB,K/12 (Item 12 from file: 348)

Method and apparatus for depositing highly oriented and reflective crystalline layers
PATENT (CC, No, Kind, Date): EP 838536 A2 980429 (Basic)
EP 838536 A3 010530
PRIORITY (CC, No, Date): US 736629 961024
ABSTRACT EP 838536 A2

The present invention is to a chemical vapor deposition process for depositing a substantially planar, highly reflective layer on a substrate 20, and is particularly useful for filling high aspect ratio holes 22 in the substrate 20 with metal-containing material. The substrate 20 is placed in a process zone 95, and successive seeding and oriented crystal growth stages are performed on the substrate. In the seeding stage, the **substrate** 20 is heated to **temperatures** Ts)) within a first lower range of **temperatures** (DELTA) Ts)), and a seeding gas is introduced into the process zone 95. The seeding gas deposits a substantially continuous, non-granular, and planar seeding layer 30 on the substrate 20. Thereafter, in an oriented crystal growth stage, the substrate 20 is maintained at deposition **temperatures** Td)) within a second higher range of **temperatures** (DELTA) TD)), and deposition gas is introduced into the process zone 95. The deposition gas forms an oriented crystal growth layer 32 on the seeding layer 30, the oriented crystal growth layer having a highly reflective surface that results from highly oriented, relatively large crystals that grow on the seeding layer.

Typically, the subroutine 148 is programmed to ramp up the temperature of the support from ambient **chamber temperatures** to a set point **temperature.** When the **substrate** reaches the seeding **temperatures** Ts)), the process gas control subroutine 146 is programmed to introduce seeding gas into the chamber, as described above. The heater control subroutine 148 also comprises an oriented crystal growth or epitaxial growth heating program code 160 for **rapidly heating** the **substrate** to deposition **temperatures** Td)) within a range of temperatures (DELTA) TD)) that are suitable for growing an oriented crystal growth layer on the seeding layer. In this step...
...the chamber manager subroutine 144a and receives a ramp rate temperature parameter of at least about 50(degree)C/min.

The heater control subroutine 148 **measures** temperature by **measuring voltage** output of a thermocouple located in the support, **compares** the **measured temperature** to the **setpoint** temperature, and increases or **decreases current** applied to the heater 80 to obtain the desired ramp rate or setpoint temperature. The temperature is obtained from the **measured voltage** by looking up the corresponding temperature in a stored conversion table, or by calculating the temperature using a fourth order polynomial.

...CLAIMS a substrate, the process comprising the steps of:
(a) placing the substrate in a process zone;
(b) in an initial seeding stage, (i) heating the **substrate** to **temperatures** Ts)) within a first lower range of temperatures (DELTA) Ts)), and (ii) introducing seeding gas into the process zone to deposit a substantially continuous seeding layer on the substrate; and
(c) in a subsequent oriented crystal growth stage, (i) maintaining the **substrate** at deposition **temperatures** Td)) within a second higher range of temperatures (DELTA) TD)), and (ii) introducing deposition gas into the process zone to form an oriented crystal growth...

28. The computer readable program product of claim 27, wherein the seeding program code means maintains the **substrate** at **temperatures** Ts)) within a range of temperatures (DELTA) Ts)) of from about 200(degree)C to about 300(degree)C.
29. The computer readable program product of claim 27, wherein the deposition program code means maintains the **substrate** at deposition **temperatures** Td)) within a range of temperatures (DELTA) TD)) of from about 200(degree)C to about 420(degree)C.

27/9/10
DIALOG(R) **File** 2:INSPEC

5894519 INSPEC Abstract Number: B9805-2550-013, C9805-3350E-026
Title: A novel method to estimate realistic losses in a multizone RTP system: a hybrid experimental-theoretical approach
Author(s): Nagabushnam, R.V.; Singh, R.K.; Sharan, S.; Sandhu, G.
Author Affiliation: Dept. of Mater. Sci. & Eng., Florida Univ., Gainesville, FL, USA
Conference **Title**: Transient Thermal Processing Techniques in Electronic Materials. Proceedings of Symposium held during the 1996 TMS Annual Meeting p.137-46
Editor(s): Ravindra, N.M.; Singh, R.K.
Publisher: TMS, Warrendale, PA, USA
Publication Date: 1996 Country of Publication: USA vii+179 pp.
ISBN: 0 87339 331 7 Material Identity Number: XX98-00491
Conference **Title**: Transient Thermal Processing Techniques in Electronic Materials. Proceedings of Symposium. Held during the 1996 TMS Annual Meeting
Conference Sponsor: TMS
Conference Date: 4-8 Feb. 1996 Conference Location: Anaheim, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Theoretical (T); Experimental (X)
Abstract: We have developed a methodology aimed at accurately determining the various forms of energy transfer (convective loss, radiative loss and absorption of lamp energy by the **wafer**) occurring in any advanced **RTP** system, based on basic system identification experiments and a simple 3D physical model depicting the heat transfer processes. The identification experiments help in the estimation of uncertain system-dependent factors which characterize the various forms of energy **transfer** , which may be otherwise difficult to calculate on a purely theoretical basis. This methodology forms the basic building block of our effort to develop a tool which can predict the temperature distribution across the **wafer** in a realistic way. **This tool can be used both as a wafer temperature control algorithm in any advanced RTP system** as well as by an end user who is equipped with a not so advanced, but **multizone, RTP system (with user defined power levels for the various zones)**.
Descriptors: convection; heat losses; heat radiation; integrated circuit **measurement**; integrated circuit testing; parameter estimation; process **control; rapid thermal processing; semiconductor** process modelling; **temperature control; temperature distribution**

27/9/12
DIALOG(R) **File** 2:INSPEC

5690461 INSPEC Abstract Number: A9720-6170A-010, B9710-2550A-015
Title: A novel technique for in-situ monitoring of crystallinity and temperature during rapid thermal annealing of thin Si/Si-Ge films on quartz/glass
Author(s): Subramanian, V.; Degertekin, F.L.; Dankoski, P.; Khuri-Yakub, B.T.; Saraswat, K.C.
Author Affiliation: Dept. of Electr. Eng., Stanford Univ., CA, USA
Conference **Title**: Flat Panel Display Materials II. Symposium p.267-72
Editor(s): Hatalis, M.K.; Kanicki, J.; Summers, C.J.; Funada, F.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1997 Country of Publication: USA xiii+513 pp.
Material Identity Number: XX97-00780
Conference **Title**: Flat Panel Display Materials II. Symposium
Conference Date: 8-12 April 1996 Conference Location: San Francisco, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Experimental (X)
Abstract: A novel technique is presented to simultaneously **measure temperature** and crystallinity in-situ during the rapid thermal **annealing** of thin Si/SiGe films on transparent substrates for active matrix liquid crystal display applications. The technique uses acoustic waves to **monitor temperature, by measuring changes in velocity with temperature**. The technique enables accurate tracking of crystalline phase transitions along with temperature, since it is independent of emissivity. **This provides a methodology for closed-loop control and end-point detection.** The experiments on thin amorphous Si on quartz demonstrate temperature repeatability of 2%. Also, the technique proved sensitive enough to detect the onset of nucleation, as evidenced by TEM. (4 Refs)
Subfile: A B
Descriptors: amorphous **semiconductors**; crystallisation; elemental **semiconductors**; emissivity; Ge-Si alloys; nucleation; **rapid thermal annealing**; **semiconductor thin films**; silicon; **temperature measurement**

27/9/21
DIALOG(R) **File** 2:INSPEC

5225907 INSPEC Abstract Number: B9605-2550-006, C9605-3350E-023
Title: A new flexible rapid thermal processing system
Author(s): Saraswat, K.C.; Chen, Y.; Degertekin, L.; Khuri-Yakub, B.T.
Author Affiliation: Dept. of Electr. Eng., Stanford Univ., CA, USA
Conference **Title**: Rapid Thermal and Integrated Processing IV. Symposium p.35-47
Editor(s): Brueck, S.R.J.; Gelpey, J.C.; Kermani, A.; Regolini, J.L.; Sturm, J.C.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1995 Country of Publication: USA xii+454 pp.
Material Identity Number: XX96-00224
Conference **Title**: Rapid Thermal and Integrated Processing IV. Symposium
Conference Date: 17-20 April 1995 Conference Location: San Francisco, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Theoretical (T)

Abstract: A highly flexible rapid thermal multiprocessing (RTM) reactor is described. This flexibility is the result of several new innovations: a lamp system, an acoustic thermometer and a **real-time control system**. The new lamp has been optimally designed through the use of a "virtual reactor" methodology to obtain the best possible **wafer** temperature uniformity. It consists of multiple concentric rings composed of light bulbs with horizontal filaments. Each ring is independently and dynamically controlled providing better control over the spatial and temporal optical flux profile resulting in excellent temperature uniformity over a wide range of process conditions. **An acoustic thermometer noninvasively allows complete wafer temperature tomography under all process conditions, a critically important measurement never obtained before. For real-time equipment and process control, a model-based multivariable control system has been developed. Extensive integration of computers and related technology for specification, communication, execution, monitoring, control, and diagnosis** demonstrates the programmability of the RTM. (12 Refs)

Subfile: B C
Descriptors: acoustic tomography; **control** system CAD; light sources ; multivariable **control** systems; process **control**; **rapid thermal processing**; real-time systems; **semiconductor** process modelling; **temperature control**; **temperature distribution**; thermometers

4/9/6 (Item 6 from file: 34)
DIALOG(R) **File** 34:SciSearch(R) Cited Ref Sci

04631574 Genuine Article#: TY246 Number of References: 125
Title: REAL-TIME OPTICAL THERMOMETRY DURING SEMICONDUCTOR PROCESSING
(REPRINTED FROM OPTICAL-DIAGNOSTICS-FOR-THIN-FILM-PROCESSING, 1996)
Author(s): HERMAN IP
Corporate Source: COLUMBIA UNIV,DEPT APPL PHYS/NEW YORK//NY/10598; COLUMBIA UNIV,COLUMBIA RADIAT LAB/NEW YORK//NY/10598
Journal: IEEE JOURNAL OF SELECTED TOPICS IN QUANTUM ELECTRONICS, **1995**, V1, N4 (DEC), P1047-1053
ISSN: 1077-260X
Language: ENGLISH Document Type: REPRINT
Geographic Location: USA
Subfile: SciSearch; CC ENGI--Current Contents, Engineering, Technology & Applied Sciences
Journal Subject Category: ENGINEERING, ELECTRICAL & ELECTRONIC; OPTICS
Abstract: The optical techniques used to **monitor the temperature of wafers** during semiconductor processing are surveyed. The physical principles underlying each method are described, Applications of each optical diagnostic are presented, along with the strengths and weaknesses of the probe, Most of these optical diagnostics have been implemented in research reactors to monitor wafer temperature during one or several types of thin-film processing, such as molecular beam epitaxy, **rapid thermal processing**, and plasma etching.

Pyrometry is the workhorse of noninvasive optical probes of temperature, although it needs **supporting models** and optical measurements to improve accuracy. Other optical thermometric wafer diagnostics are very promising and are being developed intensively, particularly reflection interferometry, transmission spectroscopy, and various interferometry methods that directly measure the thermal expansion of the wafer.
Cited References:
BARNA GG, 1994, V37, P57, SOLID STATE TECHNOL

27/9/27
DIALOG(R) **File** 2:INSPEC

4617549 INSPEC Abstract Number: B9404-2570D-011, C9404-7480-075
Title: Single-wafer processing tools for agile semiconductor production
Author(s): Moslehi, M.M.; Davis, C.J.; Paranjpe, A.; Velo, L.A.; Najm, H.N.; Schaper, C.; Breedijk, T.; Lee, Y.J.; Anderson, D.
Author Affiliation: Texas Instrum. Inc., Dallas, TX, USA
Journal: Solid State Technology vol.37, no.1 p.35-6, 38, 40-2, 44-5
Publication Date: Jan. 1994 Country of Publication: USA
CODEN: SSTEAP ISSN: 0038-111X
U.S. Copyright Clearance Center Code: 0038-111X/94/$1.00+.35
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: Total use of single-**wafer** processing for fast-cycle-time IC production avoids the high costs and rigidity of traditional batch processing. A flexible prototype single-**wafer** mini-factory contains 34 single-**wafer** processors with various combinations of process energy sources and in situ monitoring and control sensors. Forty different device fabrication processes are performed with the modular systems, most of them advanced vacuum processors (AVPs). **Vacuum cassettes transport wafers in a clean environment between machines. The AVPs are driven and supervised by a computer-integrated manufacturing (CIM) system.** Rapid thermal processing (**RTP**) AVPs have been developed for all the thermal fabrication steps required in typical 0.35- mu m CMOS technologies. Complete process integration and three-day device manufacturing cycle time have been successfully demonstrated with single-**wafer** equipment and all-**RTP** processing. (8 Refs)
Subfile: B C
Descriptors: CMOS integrated circuits; computer integrated manufacturing; computerised monitoring; electric sensing devices; fibre optic sensors; integrated circuit manufacture; **process computer control; rapid thermal** processing; **temperature control**

27/9/26
DIALOG(R) **File** 2:INSPEC

4715157 INSPEC Abstract Number: B9409-0170E-009, C9409-7410D-028
Title: **Real-time control of rapid thermal processing semiconductor manufacturing equipment**
Author(s): Schaper, C.D.
Author Affiliation: Dept. of Electr. Eng., Stanford Univ., CA, USA
p.2985-9 vol.3
Publisher: American Autom. Control Council, Evanston, IL, USA
Publication Date: 1993 Country of Publication: USA 3 vol. xxxviii+3201 pp.
ISBN: 0 7803 0860 3
Conference **Title**: Proceedings of 1993 American Control Conference - ACC '93
Conference Sponsor: IEEE; American Autom. Control Council; IFAC; et al
Conference Date: 2-4 June 1993 Conference Location: San Francisco, CA, USA
Availability: IEEE Service Center, Piscataway, NJ, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); Practical (P)
Abstract: A real-time multivariable control system has been developed for rapid thermal processing (**RTP**) **semiconductor** manufacturing equipment. The controller has been used for spatial and temporal temperature control of a **semiconductor wafer** . The control system, originally developed for prototype equipment at Stanford University, has been transferred and customized for operation on seven online **RTP** reactors at Texas Instruments. The control system has been used for more than 5000 process runs comprising 13 different thermal fabrication steps of two sub-half-micron CMOS process technologies. (0 Refs)
Subfile: B C
Descriptors: CMOS integrated circuits; integrated circuit manufacture; manufacturing computer **control**; multivariable **control** systems; **rapid thermal processing**; real-time systems; **temperature control**

27/9/23
DIALOG(R) **File** 2:INSPEC

4945866 INSPEC Abstract Number: B9506-7320R-009, C9506-3350E-019
Title: Reflexion supported **pyrometric** interferometry: A new tool for in situ, **real time temperature control in semiconductor manufacturing**
Author(s): Boebel, F.G.; Moller, H.; Preiss, W.
Author Affiliation: Fraunhofer Inst. for Integrated Circuits, Erlangen, Germany
p.130-4
Publisher: Semicond. Equipment & Mater. Int, Mountain View, CA, USA
Publication Date: 1993 Country of Publication: USA vi+253 pp.
Conference **Title**: Proceedings of 1993 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop
Conference Sponsor: IEEE; Semicond. Equipment & Mater. Int
Conference Date: 18-19 Oct. 1993 Conference Location: Boston, MA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: New Developments (N); Practical (P)
Abstract: Although temperature is one of the most important process parameters in **semiconductor** manufacturing, the **measurement** of real **wafer** temperatures has remained a very persistent problem. With new process technologies emerging-like Rapid Thermal Processing (**RTP**)-the urge for in situ, real time temperature control becomes even more demanding. In this paper we introduce reflexion supported **pyrometric** interferometry (RSPI), the first **measurement** method, which proved to be suitable for **determining the accurate surface temperature** of silicon **wafers** during film growth and other process steps without requiring knowledge about optical constants of film materials. In situ data of RSPI **measurements** during silicon oxidation are presented. RSPI is a non-intrusive, in situ temperature **measurement** method, which completely compensates for emissivity changes in the signal during the process. No material constants of the growing films have to be known and it is applicable to bare substrates as well as to single and multi-layer structures. There are no limits concerning the material composition of the coating (e.g. dielectrics are as suitable as metals). The **measurement** range is between 350 degrees C and 2000 degrees C and the temperature resolution is below 0.05 degrees C. (5 Refs)
Subfile: B C
Descriptors: elemental **semiconductors**; light interferometry; oxidation; **pyrometers**; **semiconductor** growth; **semiconductor** thin films; silicon; spectral methods of temperature **measurement**; **temperature control**

27/9/28
DIALOG(R) **File** 2:INSPEC

4519117 INSPEC Abstract Number: B9312-2550-012
Title: **Rapid thermal processing: status, problems and options after the first 25 years**
Author(s): Roozeboom, F.
Author Affiliation: Philips Res., Eindhoven, Netherlands
Conference **Title**: Rapid Thermal and Integrated Processing II **p.149-64**
Editor(s): Gelpey, J.C.; Elliott, J.K.; Wortman, J.J.; Ajmera, A.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1993 Country of Publication: USA xii424 pp.
Conference Date: 12-15 April 1993 Conference Location: San Francisco, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: General, Review (G)

Abstract: This paper reviews the current status, problems and options in **RTP** system and process design. Some commercial systems are discussed along with some improvements that can still be made in temperature reproducibility, process control and yield. This includes some recent developments in temperature reproducibility by compensated emissivity control. Uniformity issues regarding temperature and process gas hydrodynamics are highlighted in relation to reactor design. Especially in CVD applications, where radiative heat transfer may not longer dominate convective and conductive heat transfer , modeling and visualization of gas flow patterns are becoming increasingly important. Here, reactor design should be such that a laminar flow regime is reached without turbulence and without chemical memory effects upon switching to other gas compositions. Some flow visualization results are illustrated. Some new options for micro- and nanocrystallization reactions are presented before the author concludes with a technology roadmap to the 1-Gbit era. (46 Refs)

Subfile: B
Descriptors: chemical vapour deposition; flow visualisation; heat **transfer**; laminar flow; process **control; rapid thermal processing**; reviews; **semiconductor** technology; **temperature measurement**

27/9/29
DIALOG(R) **File** 2:INSPEC

4519115 INSPEC Abstract Number: B9312-7320R-013, C9312-7410H-034
Title: **In-situ temperature monitoring in RTP by acoustical techniques**
Author(s): Degertekin, F.L.; Pei, J.; Lee, Y.J.; Khuri-Yakub, B.T.; Saraswat, K.C.
Author Affiliation: E. L. Ginzton Lab., Stanford Univ., CA, USA
Conference **Title**: Rapid Thermal and Integrated Processing II p.133-8
Editor(s): Gelpey, J.C.; Elliott, J.K.; Wortman, J.J.; Ajmera, A.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1993 Country of Publication: USA xii424 pp.
Conference Date: 12-15 April 1993 Conference Location: San Francisco, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: New Developments (N); Practical (P); Experimental (X)
Abstract: A new technique utilizing the high sensitivity of acoustic wave velocity to temperature is used to **measure** the **wafer** temperature in **RTP**. Acoustic energy is coupled to a Lamb wave mode in the **wafer** using the quartz support pins already present in most rapid thermal processors. The tips of the pins are sharpened to have point contact with the **wafer** and acoustic transducers are bonded to the other **end** to excite and detect acoustic waves. By **measuring** the pin-to-pin time of flight of Lamb waves, it is possible to monitor the **wafer** temperature in-situ in the 20-1000 degrees C range with+or-5 degrees C accuracy. Increasing SNR to 50 dB by spring loading the pins and using better electronics, it is possible to improve this figure to+or-1 degrees C. Also a modified system with multiple spring loaded pins is constructed and **wafer** temperature mapping is performed using tomographic reconstruction techniques. The resulting images are in good agreement with thermocouple readings and can be used for temperature control and rapid thermal processor design. (4 Refs)
Subfile: B C
Descriptors: computerised monitoring; computerised tomography; integrated circuit manufacture; **rapid thermal processing**; **semiconductor** technology; surface acoustic wave devices; **temperature control**; **temperature measurement**; **ultrasonic applications**

27/9/31
DIALOG(R) **File** 2:INSPEC

03860146 INSPEC Abstract Number: B91024217, C91031838
Title: A global model for rapid thermal processors
Author(s): Sorrell, F.Y.; Harris, J.A.; Gyurcsik, R.S.
Author Affiliation: North Carolina State Univ., Raleigh, NC, USA
Journal: IEEE Transactions on Semiconductor Manufacturing vol.3, no.4 p.183-8
Publication Date: Nov. 1990 Country of Publication: USA
CODEN: ITSMED ISSN: 0894-6507
U.S. Copyright Clearance Center Code: 0894-6507/90/1100-0183$01.00
Language: English Document Type: Journal Paper (JP)
Treatment: Applications (A); Theoretical (T)
Abstract: A simple model for the components that make up a rapid thermal processing system is given. These components are the furnace, the **pyrometer used to measure temperature, and the control system that utilizes the pyrometer measurement to control the power to the lamps**. The models for each of the components are integrated in a numerical code to give a computer simulation of the complete furnace operation. The simulation can be used to investigate the interaction of the furnace, temperature-sensing technique, and the control system. Therefore, the interplay of heat transfer (furnace) properties, optical (**pyrometer**) parameters, and control gains can be studied. The objective is to **define variability in wafer temperature as process parameters change**. The following three applications of the model are included: (1) a simulation of open-loop operation; (2) a simulation of the ramp up and subsequent operation with a step change in **wafer** optical properties; and (3) a simulation of the rapid thermal chemical vapor deposition of polysilicon on silicon oxide which demonstrates the applicability model for actual processes. A technique for correction of **pyrometer** output to improve temperature control is also presented. (13 Refs)
Subfile: B C
Descriptors: **annealing**; chemical vapour deposition; **control** systems; digital simulation; feedback; **heat treatment**; modelling; **pyrometers**; **semiconductor** technology; **temperature control**

45/9/11
DIALOG(R) **File** 2:INSPEC

3966096 INSPEC Abstract Number: B91056061, C91061065
Title: **Automatic problem detection and documentation in a plasma etch reactor**
Author(s): Barna, G.G.
Author Affiliation: Texas Instrum. Inc., Dallas, TX, USA
Conference **Title**: Ninth IEEE/CHMT International Electronic Manufacturing Technology Symposium. Competitive Manufacturing for the Next Decade. Proceedings 1990 IEMT Symposium (Cat. No. 90CH2864-7) p.47-50
Publisher: IEEE, New York, NY, USA
Publication Date: 1990 Country of Publication: USA x+370 pp.
U.S. Copyright Clearance Center Code: CH2864-7/90/0000-0047$01.00
Conference Sponsor: IEEE
Conference Date: 1-3 Oct. 1990 Conference Location: Washington, DC, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: IC manufacturing involves a large number of complex process steps. There is a probability of a microprocessing error in each of these steps. The author describes two software tools, in a single-wafer plasma etcher, that have been developed to minimize the occurrence and maximize the efficiency of the diagnosis of such microprocessing. The first examines the endpoint trace of every wafer and determines whether that wafer has seen anomalous processing. If so, **the software can terminate the processing of subsequent wafers**. The second records the analog values of all the **process control parameters** during the entire etch process. When these two routines are linked appropriately, it is possible to record these analog values for only those wafers that have seen anomalous processing. This feature provides data for the analysis of the process problem. These procedures thus act to minimize the number of wafers that are microprocessed and provide pertinent diagnostic information for those that have been. (4 Refs)
Subfile: B C
Descriptors: computerised monitoring; integrated circuit manufacture; manufacturing data processing; **semiconductor** device manufacture; sputter etching; statistical process control

33/9/6
DIALOG(R) **File** 2:INSPEC

03612645 INSPEC Abstract Number: B90028563
Title: Limited reaction processing: growth of Si/sub 1-x/Ge/sub x//Si for heterojunction bipolar transistor applications
Author(s): Hoyt, J.L.; King, C.A.; Noble, D.B.; Gronet, C.M.; Gibbons, J.F.; Scott, M.P.; Laderman, S.S.; Rosner, S.J.; Nauka, K.; Turner, J.; Kamins, T.I.
Author Affiliation: Stanford Electron. Labs., CA, USA
Journal: Thin Solid Films vol.184 p.93-106
Publication Date: Jan. 1990 Country of Publication: Switzerland
CODEN: THSFAP ISSN: 0040-6090
U.S. Copyright Clearance Center Code: 0040-6090/90/$3.50
Conference **Title**: 3rd International Symposium on Silicon Molecular Beam Epitaxy, Symposium A of the 1989 E-MRS Conference
Conference Date: 30 May-2 June 1989 Conference Location: Strasbourg, France
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Experimental (X)
Abstract: Limited reaction processing (LRP) of silicon-based materials is reviewed as an alternative growth method to molecular beam epitaxy (MBE). LRP is a chemical vapor deposition technique which **uses wafer temperature**, rather than gas flow switching, **to initiate and terminate growth**. Processing takes place within a cold-wall, quartz reaction chamber, and gases are changed between successive lamp-heated growth cycles. In addition to minimizing thermal exposure, the technique allows individual layers in a multi-layer structure to be deposited at their optimum growth temperature. LRP is particularly well suited to the growth and processing of metastable layers such as strained Si/sub 1-x/Ge/sub x/ on silicon. Several properties of LRP-grown Si/sub 1-x/Ge/sub x/ are shown to be similar to those reported for MBE material, including qualitative islanding behavior and quantitative measurement of the onset of misfit dislocation formation. However, a direct comparison of thermal stability reveals larger numbers of misfit dislocations in MBE-grown films upon **annealing** . The electrical behavior of misfit dislocations in heterojunction diodes, and the growth and analysis of high-quality Si/Si/sub 1-x/Ge/sub x//Si heterojunction bipolar transistors are also discussed. (27 Refs)
Subfile: B
Descriptors: chemical vapour deposition; dislocations; elemental semiconductors; Ge-Si alloys; heterojunction bipolar transistors; silicon

27/9/32
DIALOG(R) **File** 2:INSPEC

03830737 INSPEC Abstract Number: B91016629
Title: RTP cluster tool module with integrated temperature control system
Journal: Solid State Technology vol.33, no.8 p.39-41
Publication Date: Aug. 1990 Country of Publication: USA
CODEN: SSTEAP ISSN: 0038-111X
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: Peak's **RTP** cluster module brings the advantages of cold wall vacuum processing and integrated temperature control with automatic compensation of emissivity to the multiprocessing environment providing true integration of **RTP** into production. Because the module is identical to the one used in standalone **RTP** equipment, the development and transfer of processes for **wafers** up to 200 mm diam. to the cluster environment is simplified. The door is open not only to the clustering of **RTP** with deposition and etch but also to multichamber rapid thermal processing systems. (0 Refs)
Subfile: B
Descriptors: **incoherent light annealing**; **integrate**d circuit manufacture; modules; **semiconductor** technology; **temperature control**

33/9/7
DIALOG(R) File 2:INSPEC

03580519 INSPEC Abstract Number: A90040505, B90021454
Title: A model for the silicon wafer bonding process
Author(s): Stengl, R.; Tan, T.; Gosele, U.
Author Affiliation: Sch. of Eng., Duke Univ., Durham, NC, USA
Journal: Japanese Journal of Applied Physics, Part 2 (Letters) vol.28, no.10 p.1735-41
Publication Date: 1989 Country of Publication: Japan
CODEN: JAPLD8 ISSN: 0021-4922
Language: English Document Type: Journal Paper (JP)
Treatment: Experimental (X)
Abstract: The bonding speed (or contact wave velocity) of silicon and fused quartz **wafers** has been measured as a function of temperature. The results show that the bonding **process stops to operate at temperatures above 90 degrees C and 320 degrees C for fused quartz and bare silicon wafers, respectively**. By comparing their results to infrared spectra obtained from silica gel the authors develop a tentative model of the bonding process. This model is based on the assumption that the initial **wafer** bonding process occurs via hydrogen bonds of adsorbed water. This model **explains why the bonding strength increases in two distinct steps during high temperature annealing** . By introducing a phenomenological time constant tau they can also account for the fact that in an intermediate temperature range the bonding strength does not depend on **annealing** time as it has been reported in the literature.
Subfile: A B
Descriptors: annealing; elemental semiconductors; hydrogen bonds; semiconductor technology; silicon

73/TI,PN,PD,AN,AD,IC,AB,AB,K/4 (Item 4 from file: 348)
DIALOG(R) File 348:**(c)** European Patent Office.
Single frequency adapter for laser.
PATENT (CC, No, Kind, Date): EP 334403 A1 890927 (Basic)
EP 334403 B1 931222
PRIORITY (CC, No, Date): US 172262 880323
ABSTRACT EP 334403 A1
A single frequency adapter for a gas laser comprises a jacket (11) for engaging and being secured to the casing (10) surrounding the gas laser (15), an induction coil (20) fixed within said jacket and positioned to surround the hollow mirror mount (18) at one end of the laser tube while being outwardly spaced from the hollow mount, a means (Vb) for applying an alternating current to the induction coil, and means (Q1) for modulating the current in the induction coil.

...SPECIFICATION
An oscillator comprised of inverting amplifier A4 drives the transistor Q1 at a frequency in the vicinity of 1 MHz. **The leads from a thermocouple TC are applied to OP AMP A1. This signal is compared to a temperature reference signal in comparator M1. Until the feedback reference signal exceeds the reference, it controls the error amplifier comprising OP AMP A3 so that the amplitude of the signal applied to the gate of transistor Q1 is not attenuated. As soon as the desired temperature is reached, the output 11 the comparator M1 goes positive and current ceases to flow in the circuit of diode D1**. At this time the laser power control begins. The output from the PIN diode 26 is applied to OP AMP A2. The amplified feedback signal is applied to the error amplifier A3 where it is **compared** with a **reference** signal taken at potentiometer P.

27/9/35
DIALOG(R) **File** 2:INSPEC

2222954 INSPEC Abstract Number: B84019875
Title: Laser **annealing** of **semiconductor** devices
Author(s): Hill, C.
Author Affiliation: Allen Clark Res. Centre, Plessey Res. (Caswell) Ltd., Towcester, UK
Conference **Title**: Physical Processes in Laser-Materials Interactions. Proceedings of the 1980 NATO Advanced Study Institute p.221-9
Editor(s): Bertlotti, M.
Publisher: Plenum, New York, NY, USA
Publication Date: 1983 Country of Publication: USA xi+521 pp.
ISBN: 0 306 41107 5 Material Identity Number: XX83-01703
Conference Date: 13-25 July 1980 Conference Location: Pianore, Italy
Language: English Document Type: Conference Paper (PA)
Treatment: General, Review (G); Theoretical (T)
Abstract: Conventional isothermal heat treatment techniques have served for **semiconductor** fabrication very well up until now. Most of the physical processes involved in fabrication are rate-determined by a solid state diffusion process (e.g. oxidation, dopant redistribution, anneal of implantation damage) and such processes have activation energies typically in the range 2-5 eV. The resulting sensitivity to temperature has required temperature control to +or-1 degrees C on modern **semiconductor furnaces**, and this is routinely met. What, then, is the place of radiant beam processing? This technique opens up the possibility of non-isothermal heat treatment, in which one has **control over the spatial and temporal extent of the temperature profile inside the silicon over a very wide range of times (100 picosecs to 100 secs) and distances (0.1 micron to 1000 microns). This selectivity and control of beam annealing makes completely new types of processing possible**, and the purpose of this paper is to examine these new possibilities in the light of their usefulness for device fabrication and particularly for silicon integrated circuit processing. (43 Refs)
Subfile: B
Descriptors: elemental **semiconductors**; integrated circuit technology; laser beam **annealing**; **semiconductor** device manufacture; **semiconductor** devices; **semiconductor** technology; silicon